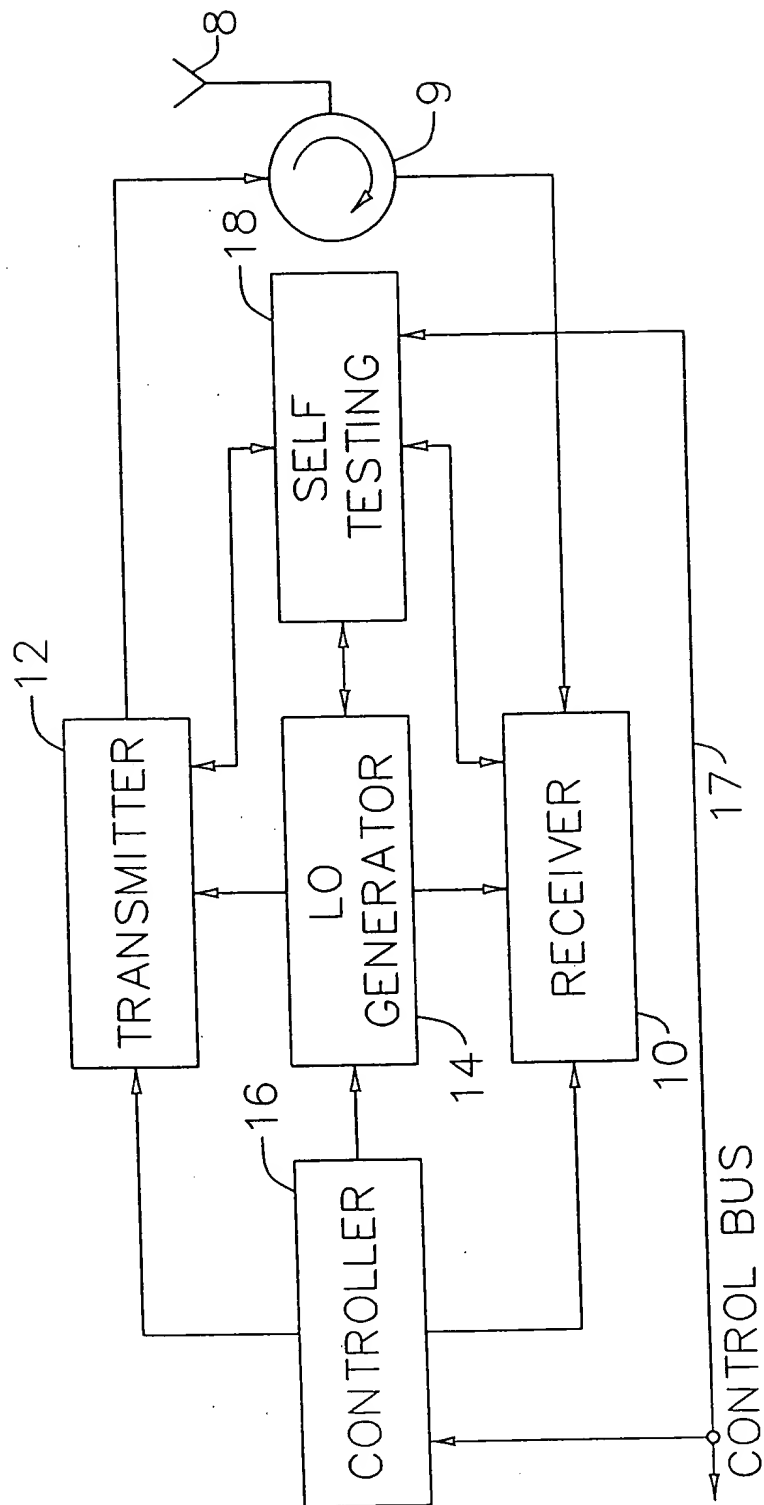


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FIG. 1



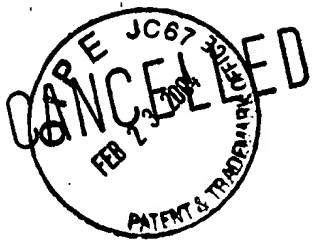
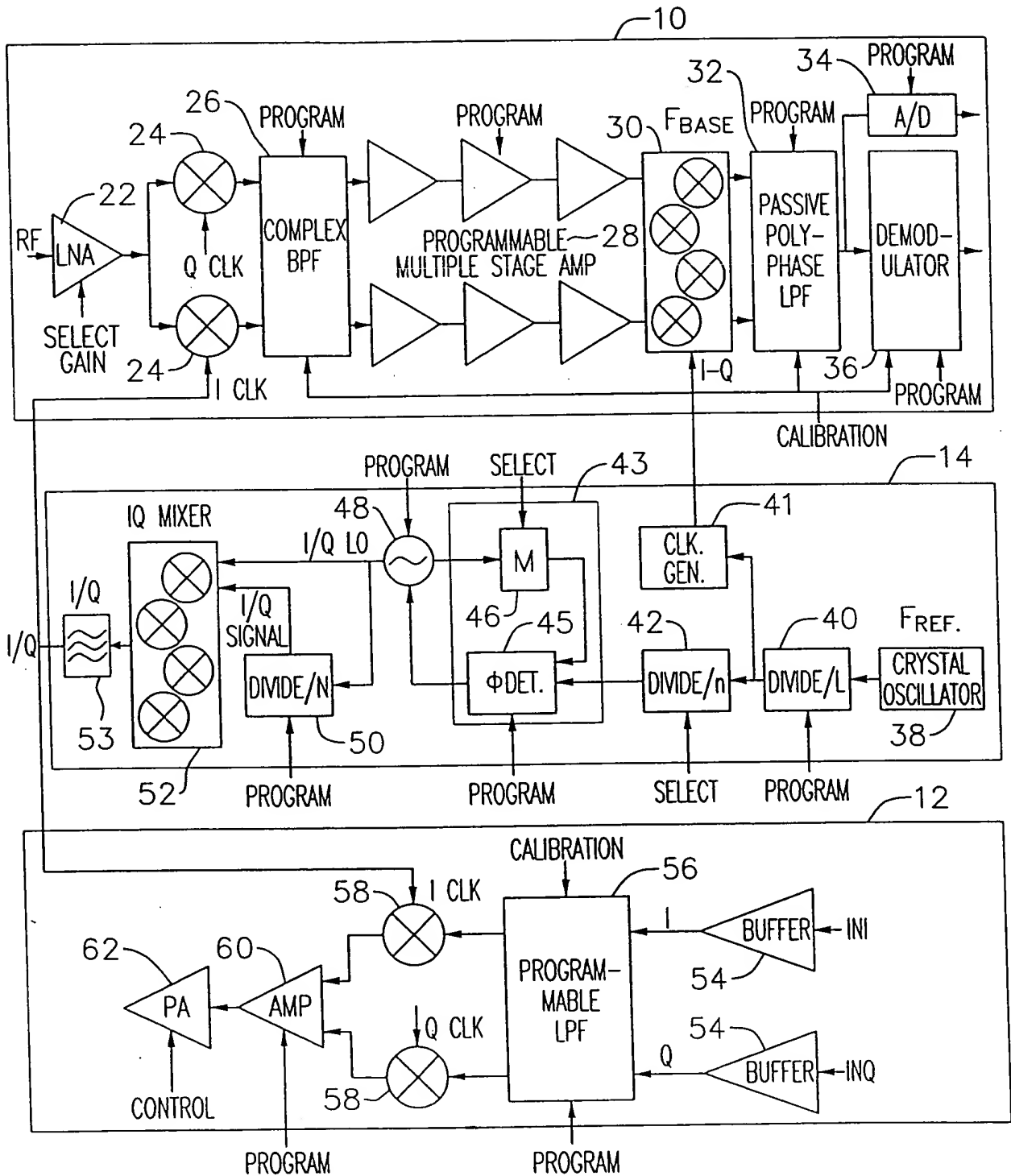


FIG. 2



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FIG. 3

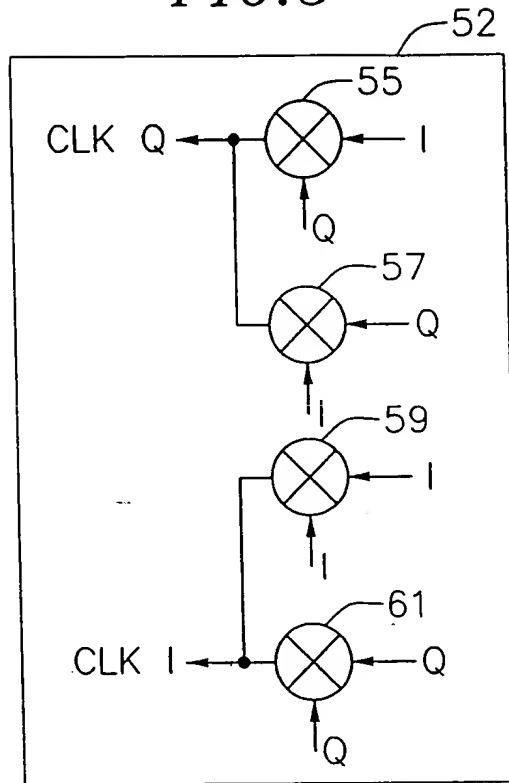
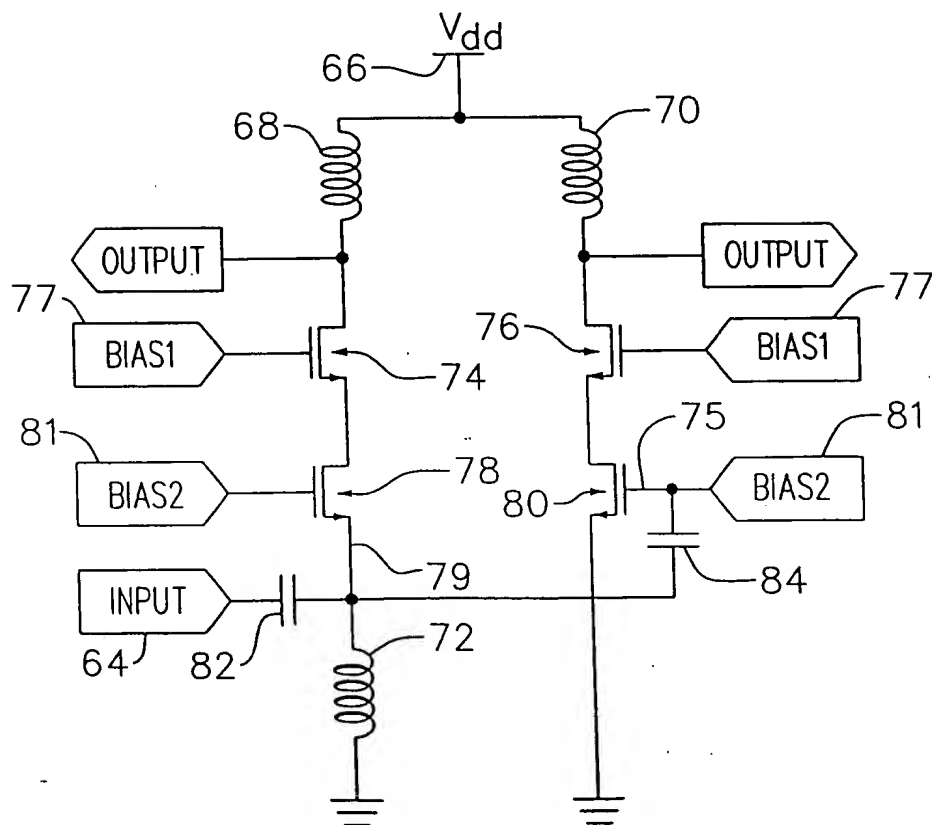


FIG. 4

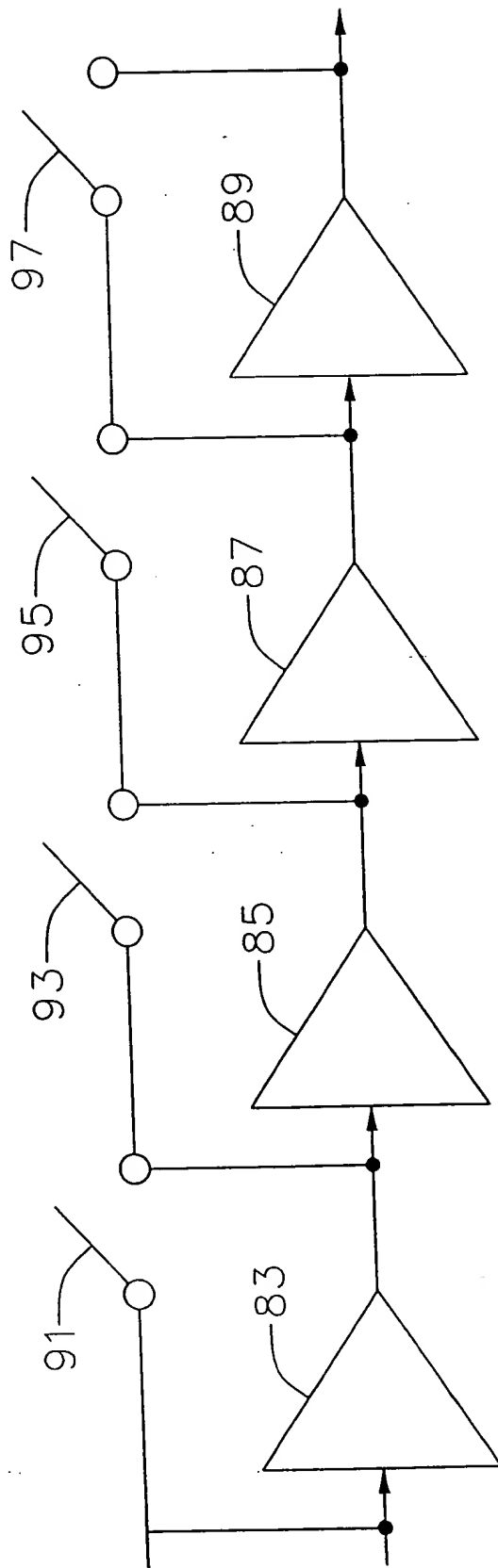




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FIG. 5



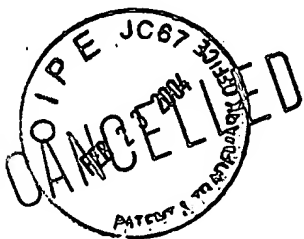
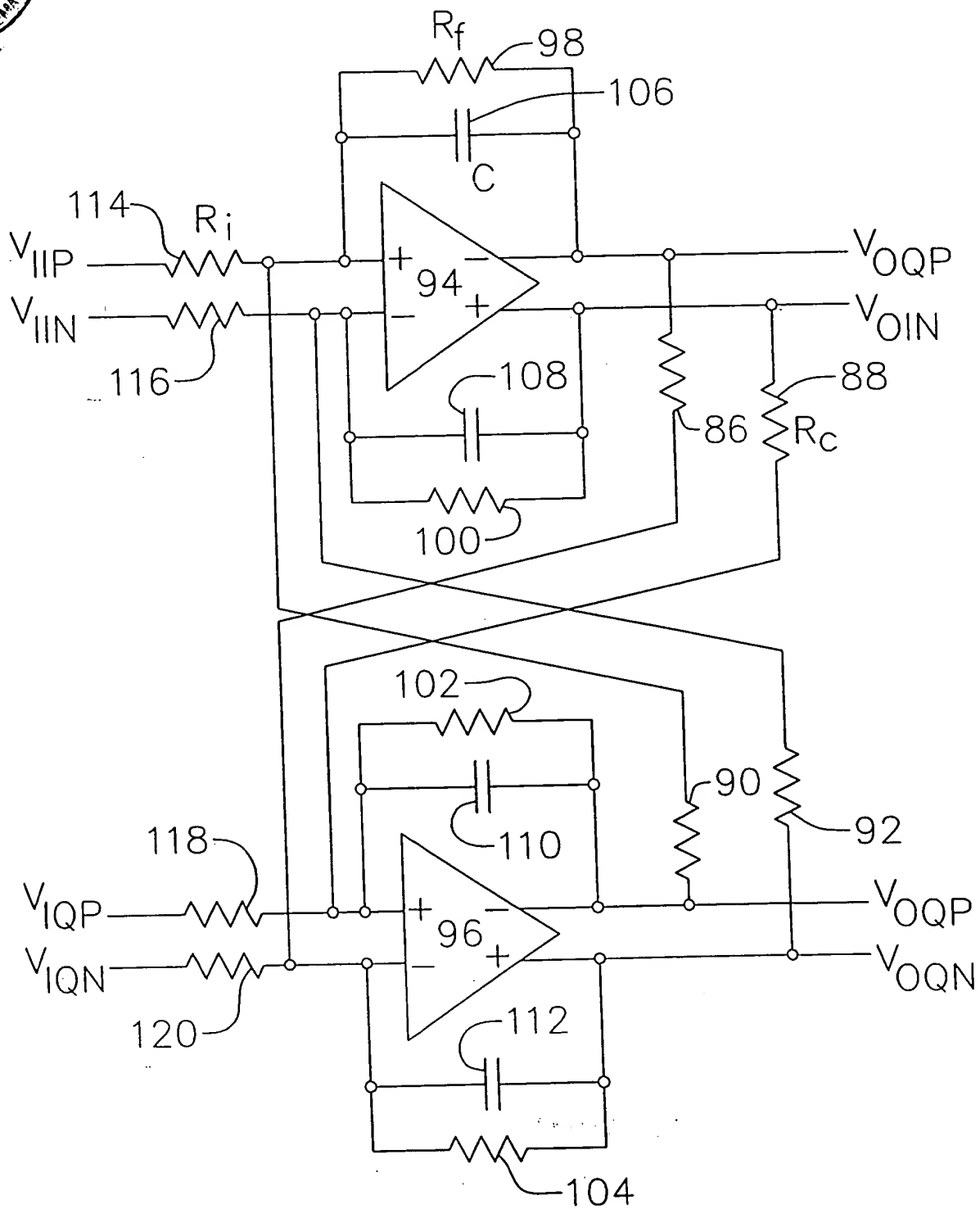


FIG. 6



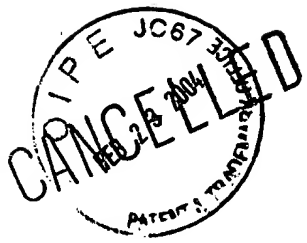


FIG. 7

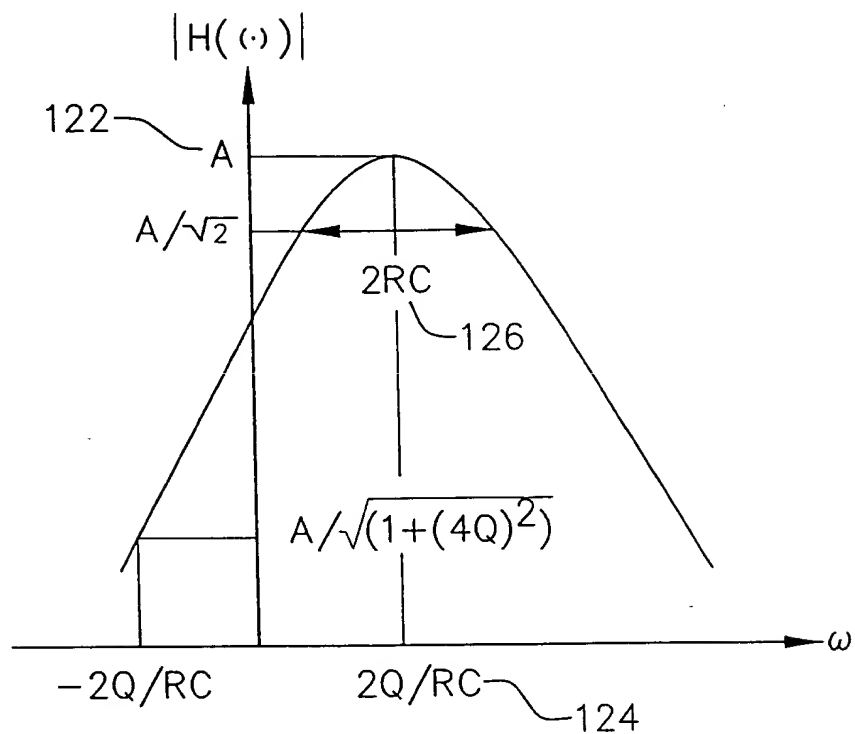


FIG. 8

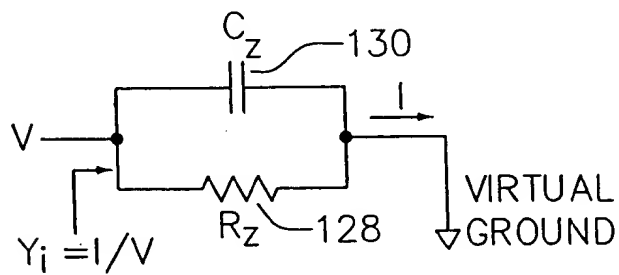
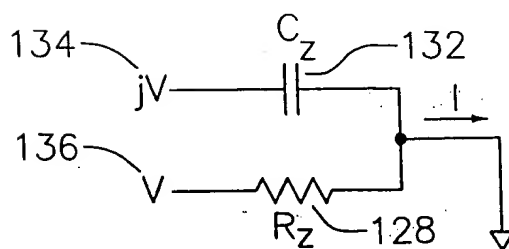


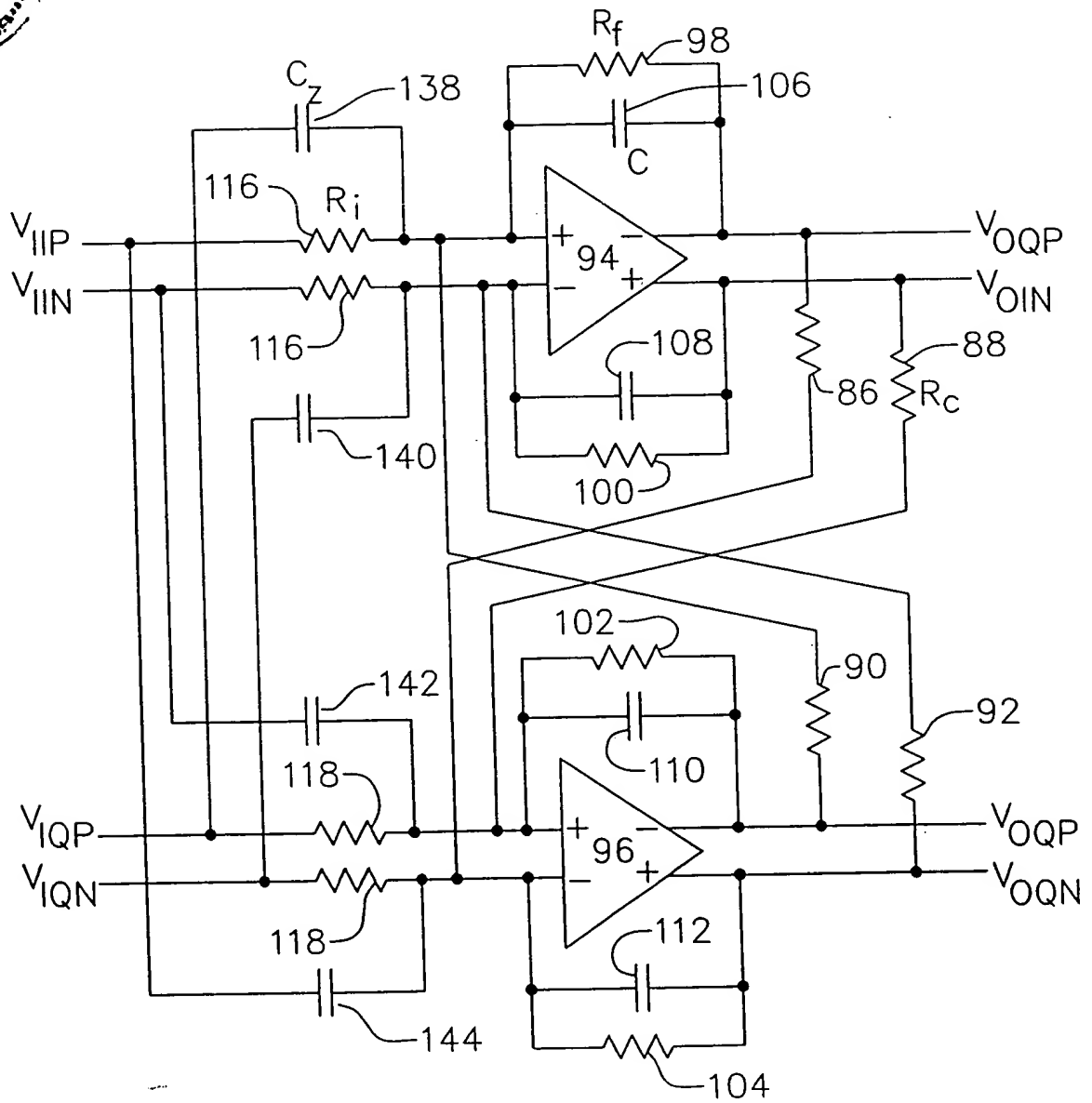
FIG. 9



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FIG. 10



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FIG. 11

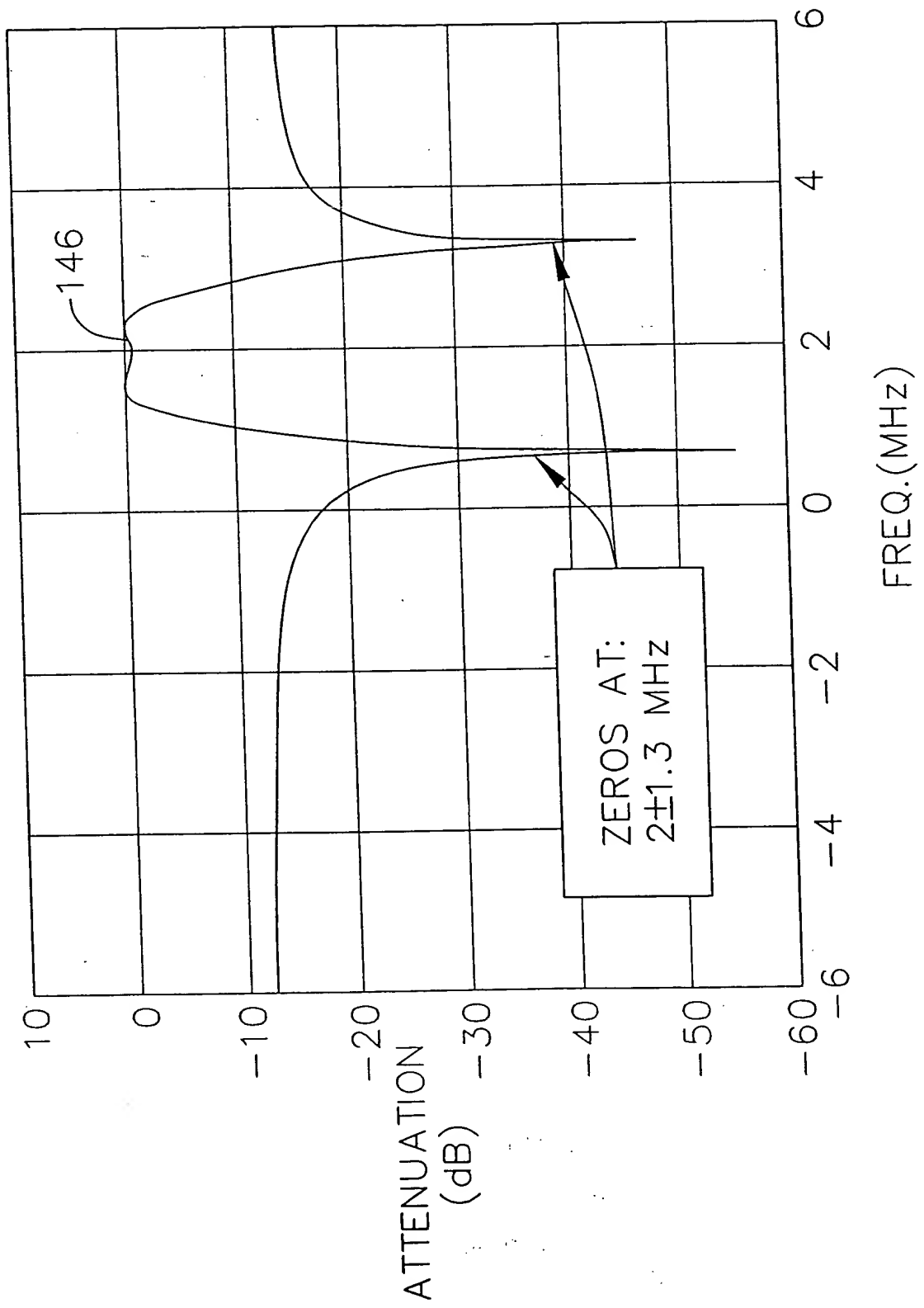




FIG. 12(a)

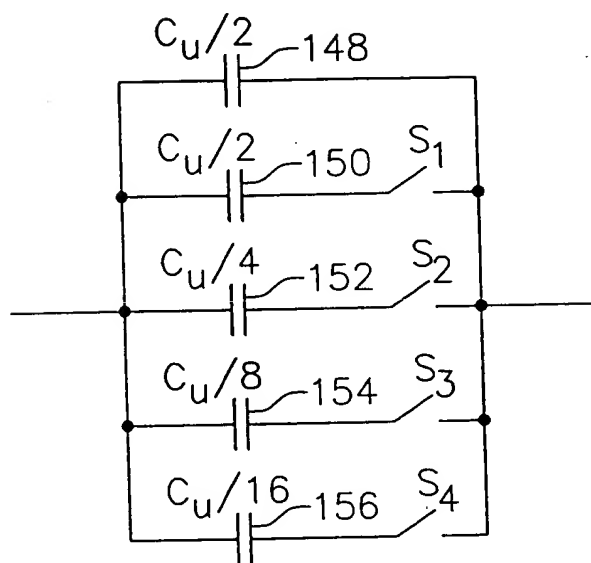
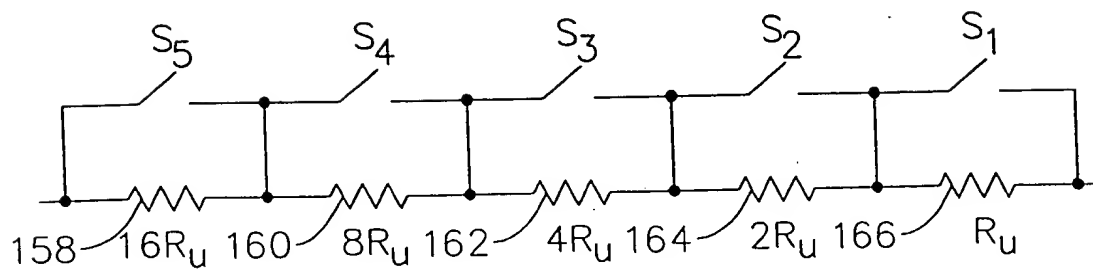


FIG. 12(b)



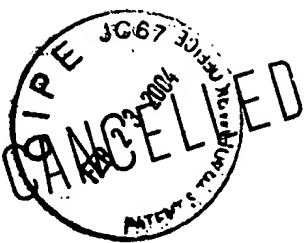


FIG. 13

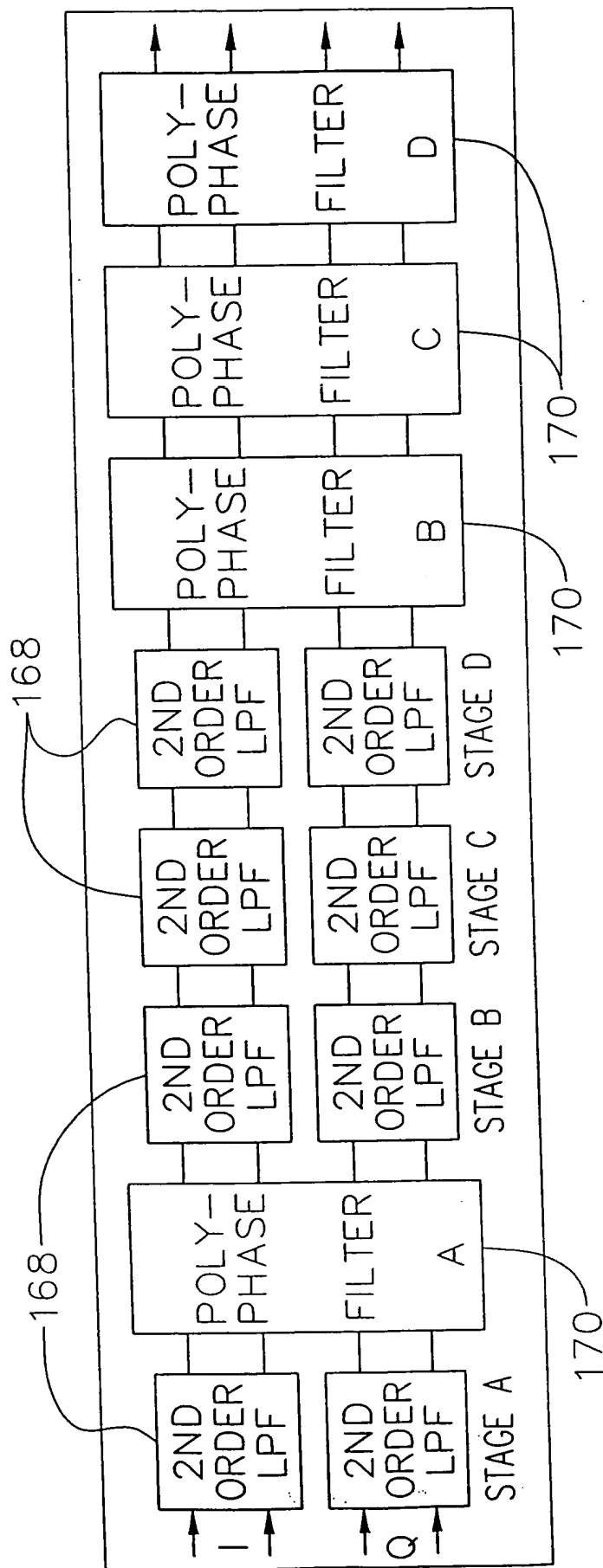
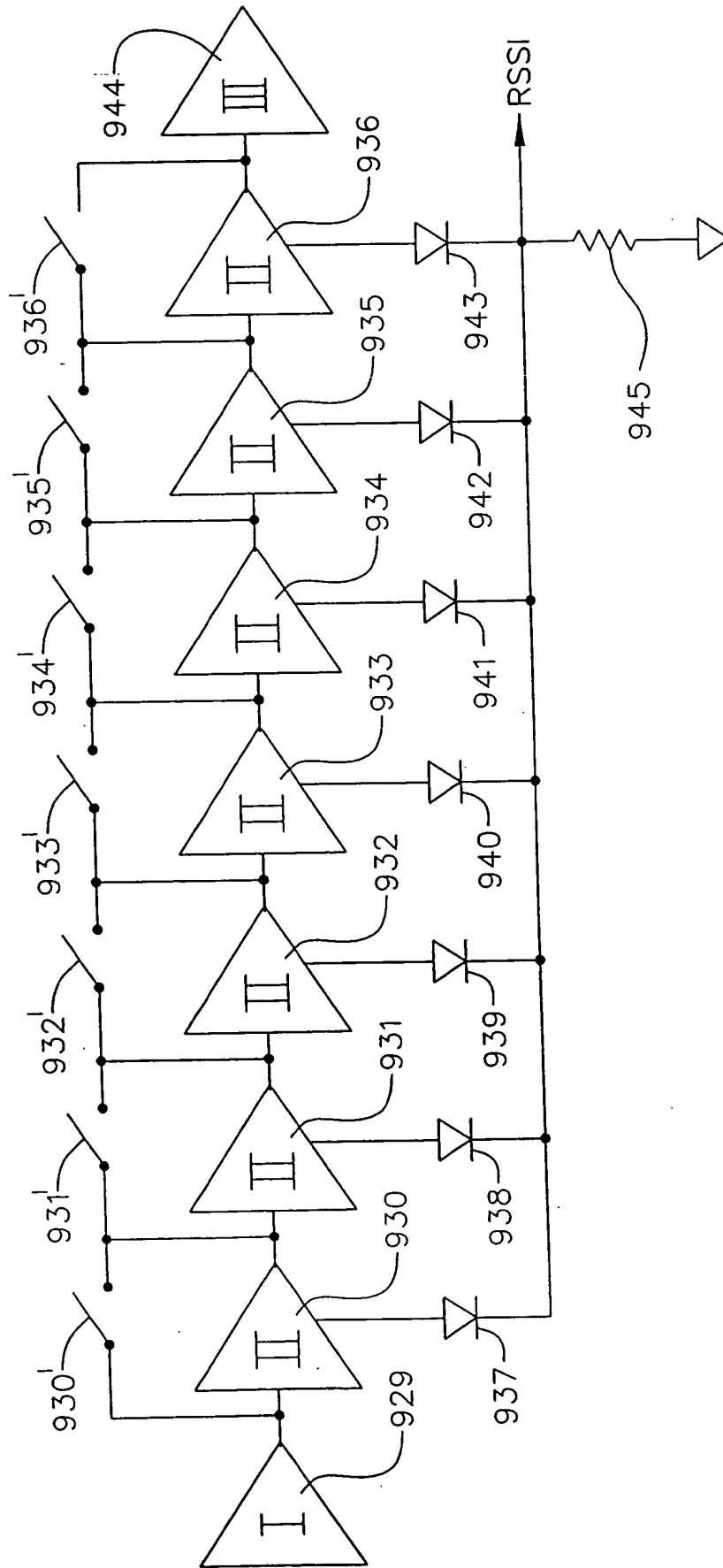




FIG. 14



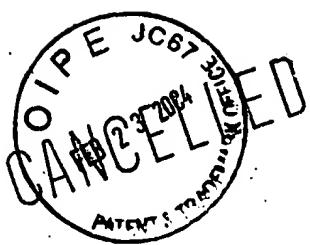


FIG. 15

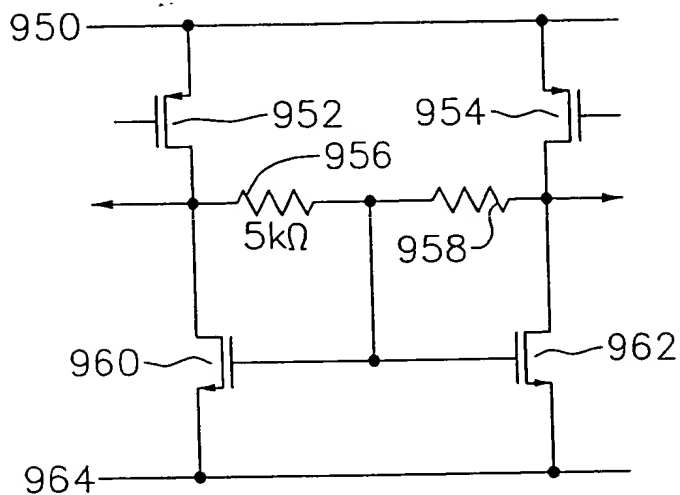
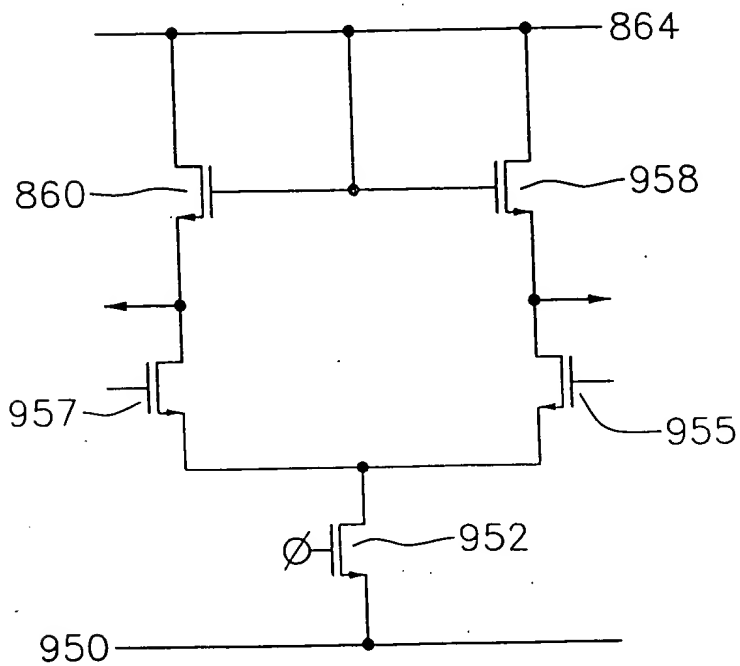


FIG. 16(a)



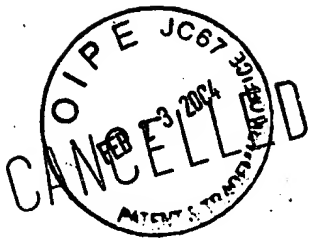
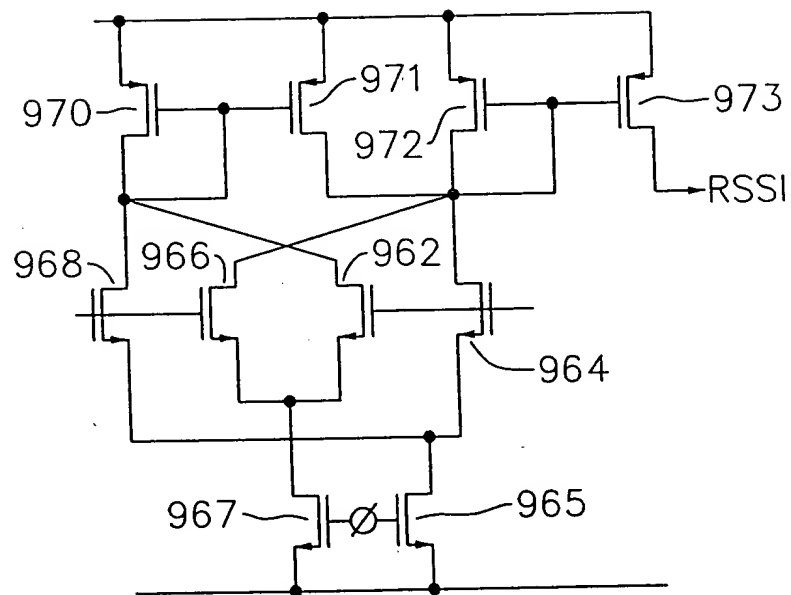


FIG. 16(b)



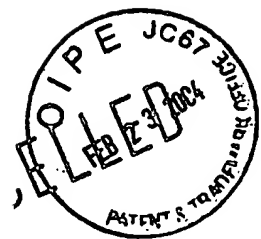


FIG.17(a)

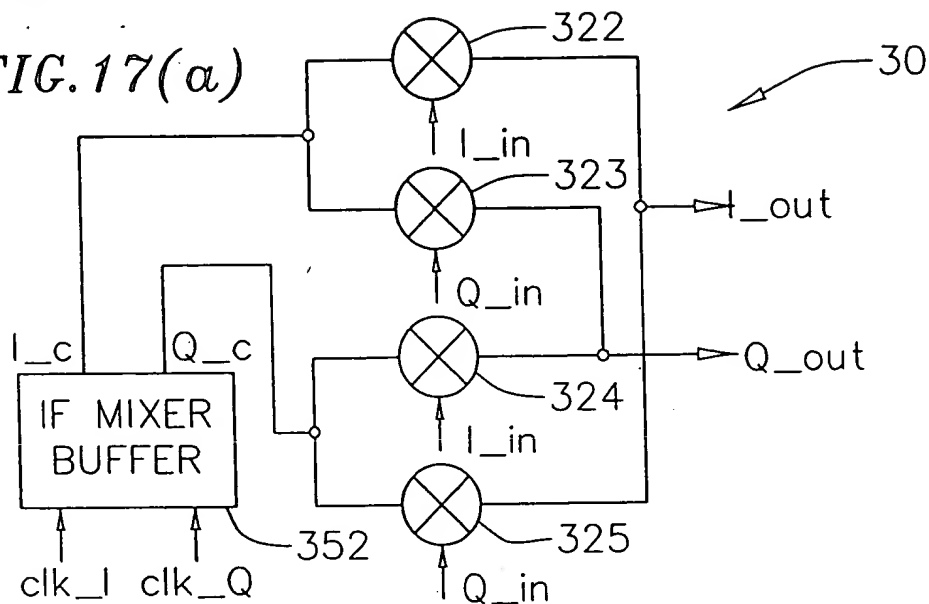


FIG.17(b)

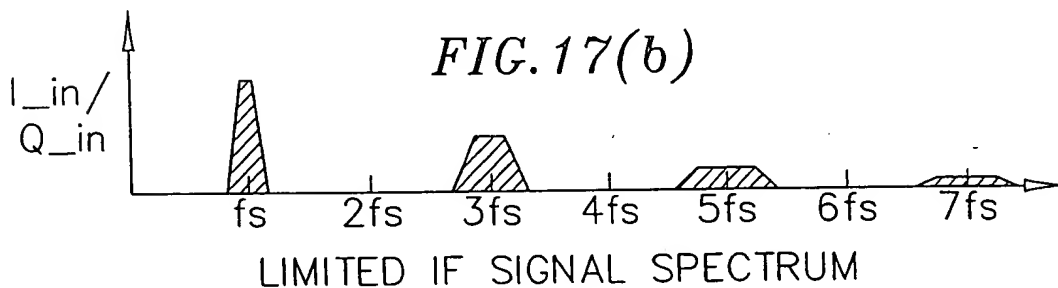


FIG.17(c)

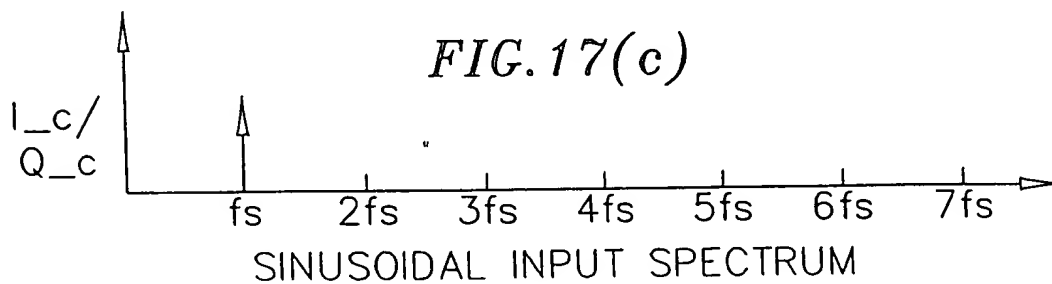
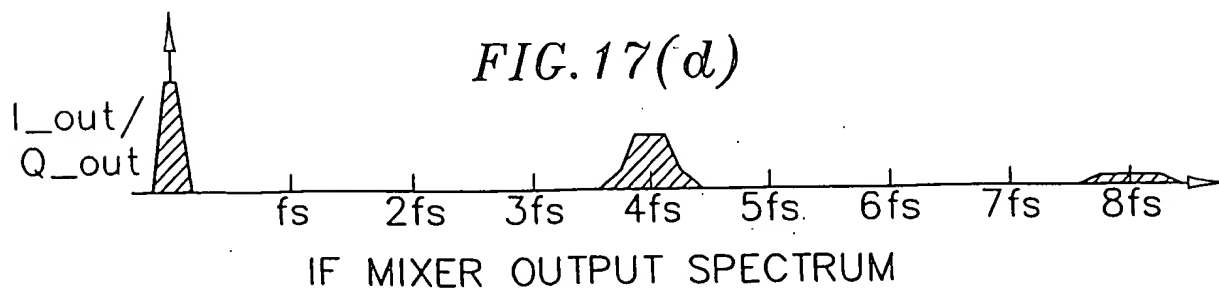


FIG.17(d)



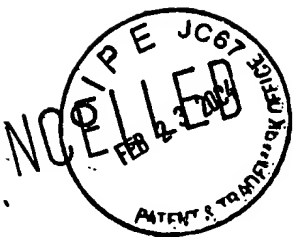


FIG. 18

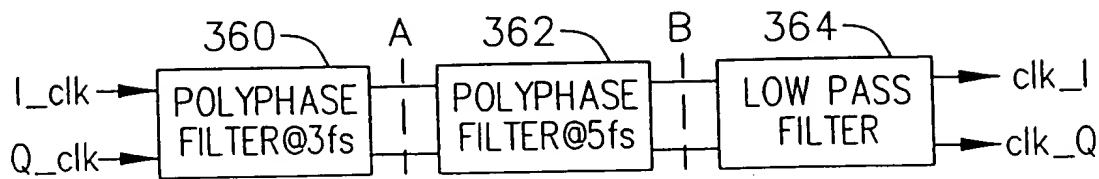


FIG. 19(a)

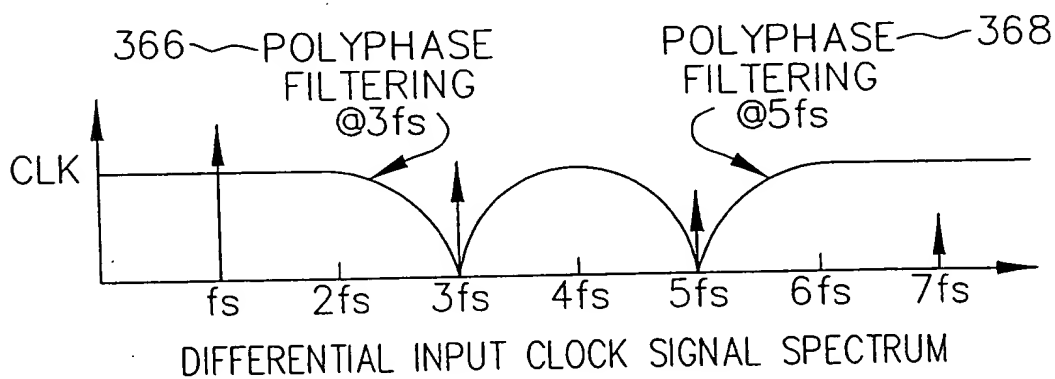


FIG. 19(b)

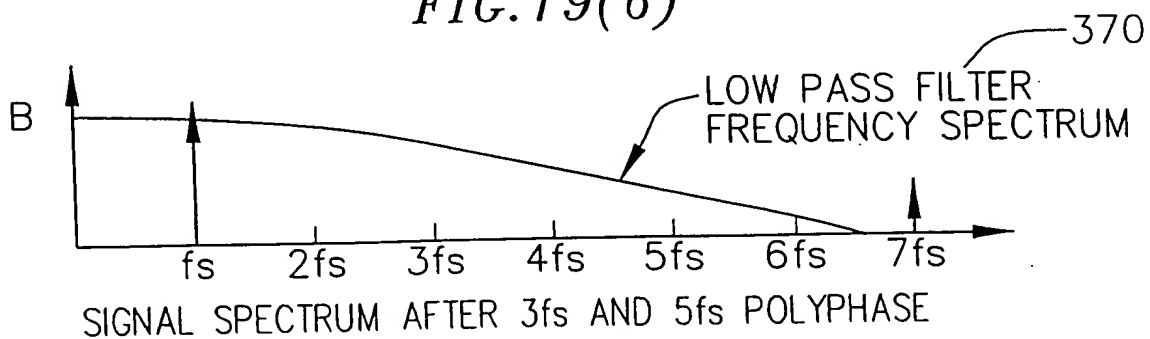
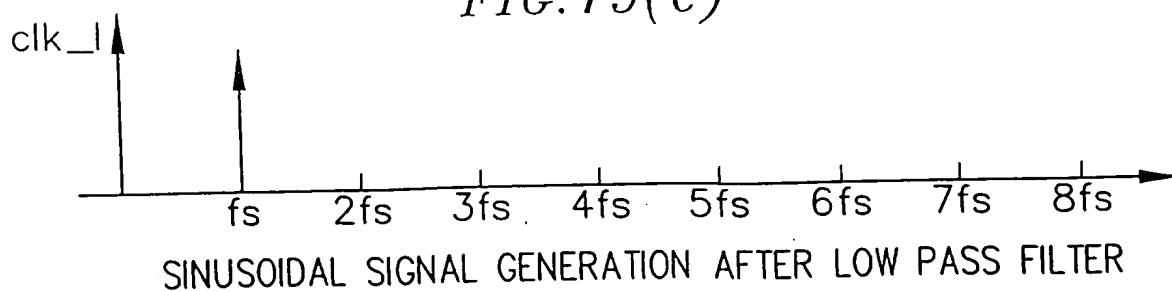


FIG. 19(c)



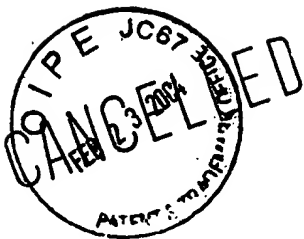


FIG.20(a)

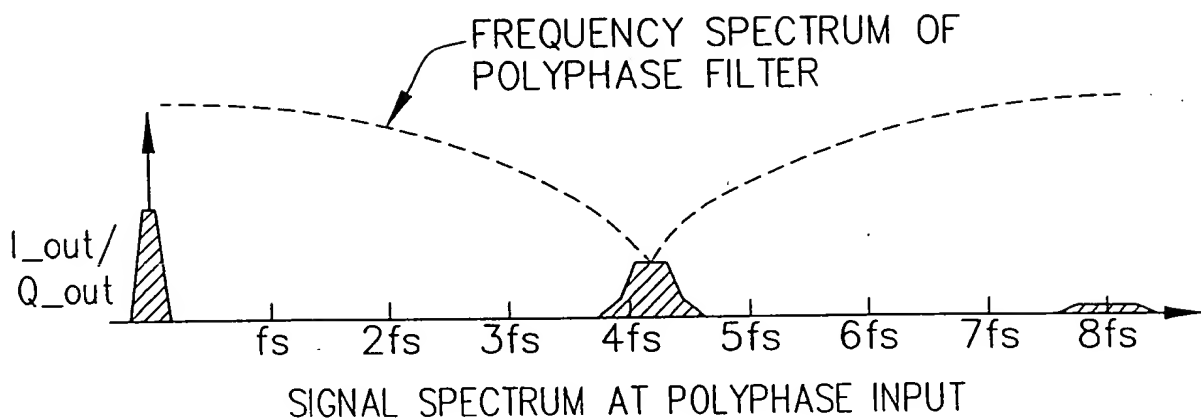


FIG.20(b)

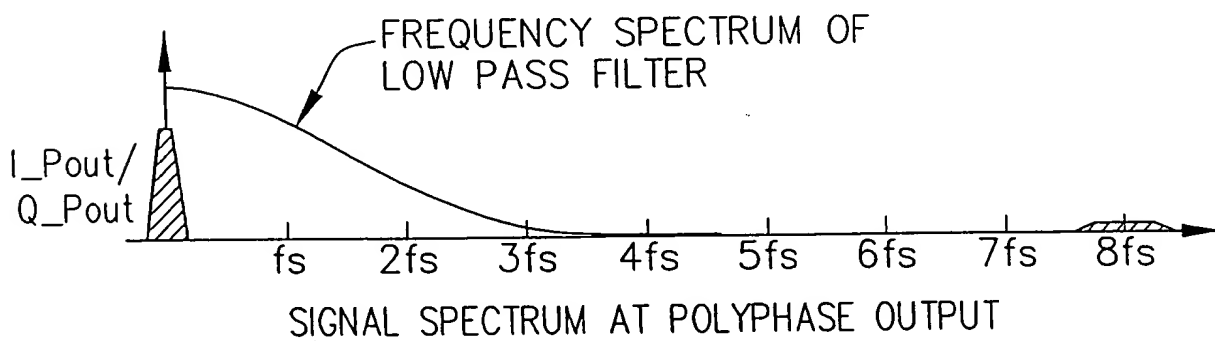
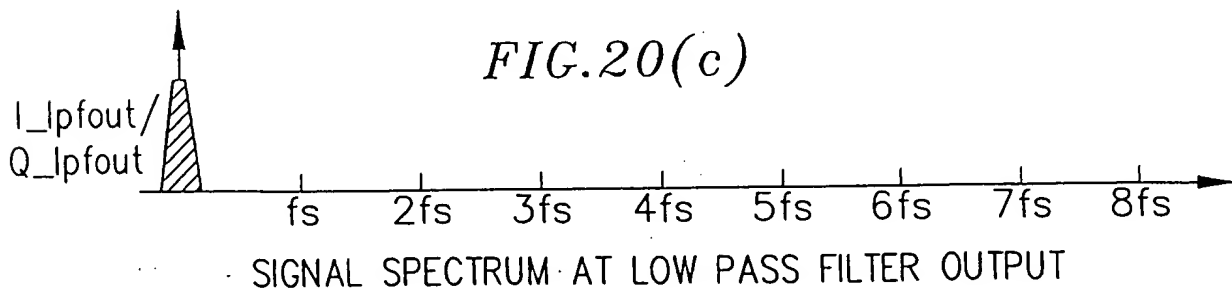


FIG.20(c)



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FIG.21

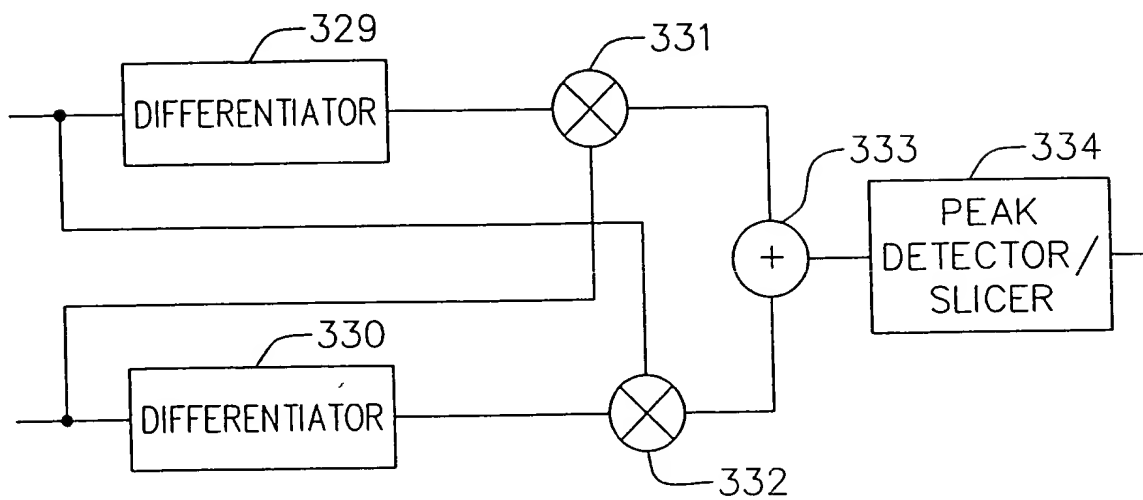
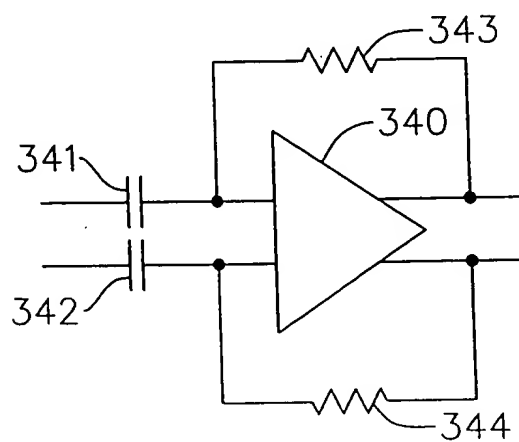


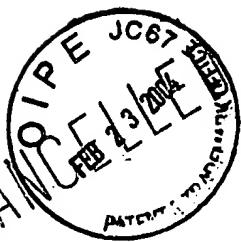
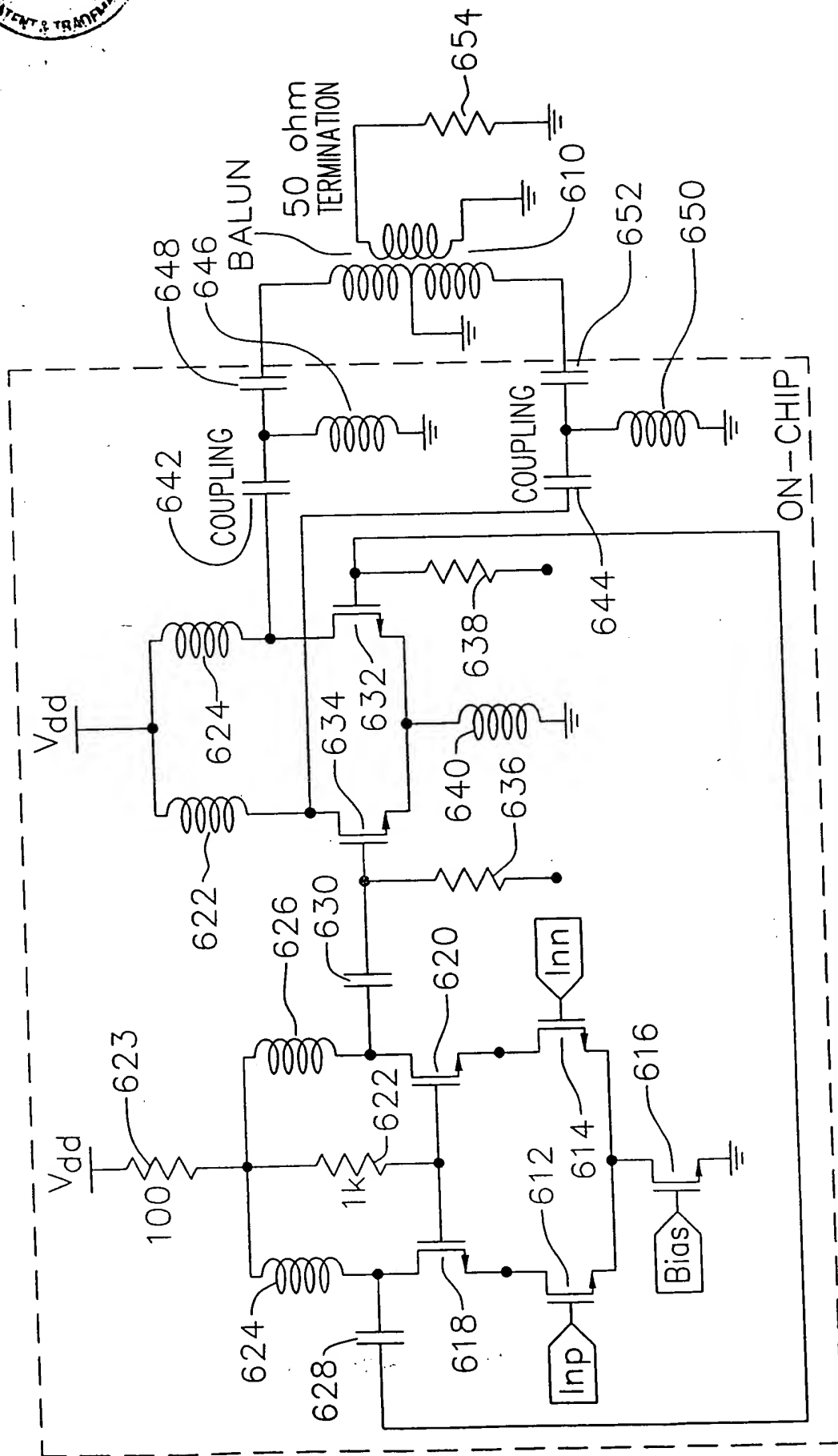
FIG.22





The diagram shows a differential amplifier circuit. It features two input lines at the top. The first input line is connected to the non-inverting input of a large triangular amplifier block labeled 345. The second input line is connected to the inverting input of the same amplifier block. A feedback path is formed by two resistors, 348 and 349, connected in series between the output of the amplifier (345) and its inverting input. Two rectangular blocks labeled 'PEAK DETECTOR' are present. The first peak detector (346) has its inputs connected to the first and second input lines and its output connected to the inverting input of the amplifier. The second peak detector (347) has its inputs connected to the first and second input lines and its output connected to the junction between resistors 348 and 349. The output of the amplifier (345) is connected to a logic gate structure labeled 350, which consists of an inverter followed by a buffer.

FIG. 25



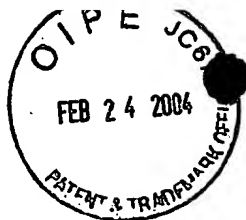
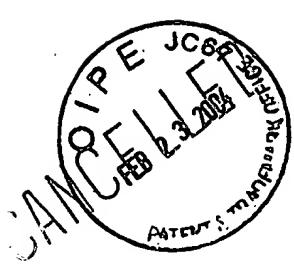


FIG.26(a)

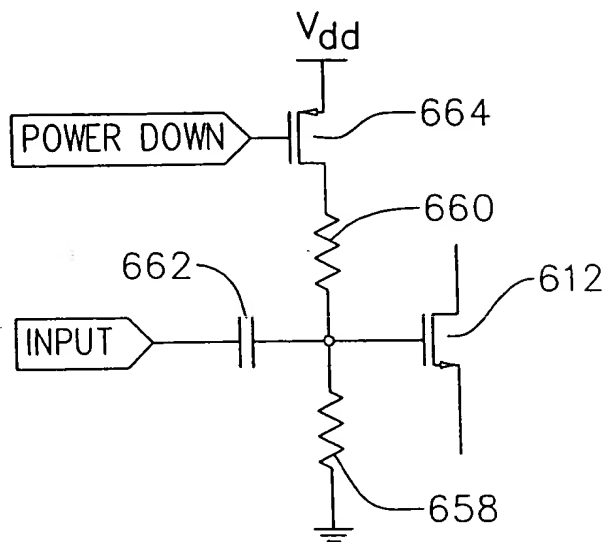


FIG.26(b)

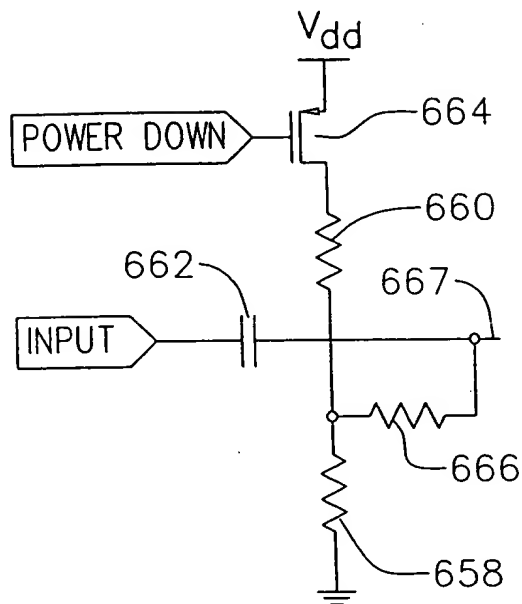


FIG.27

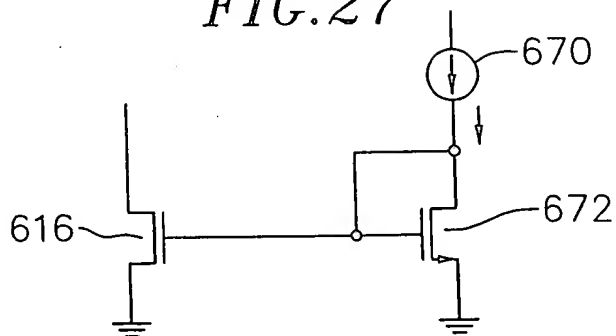
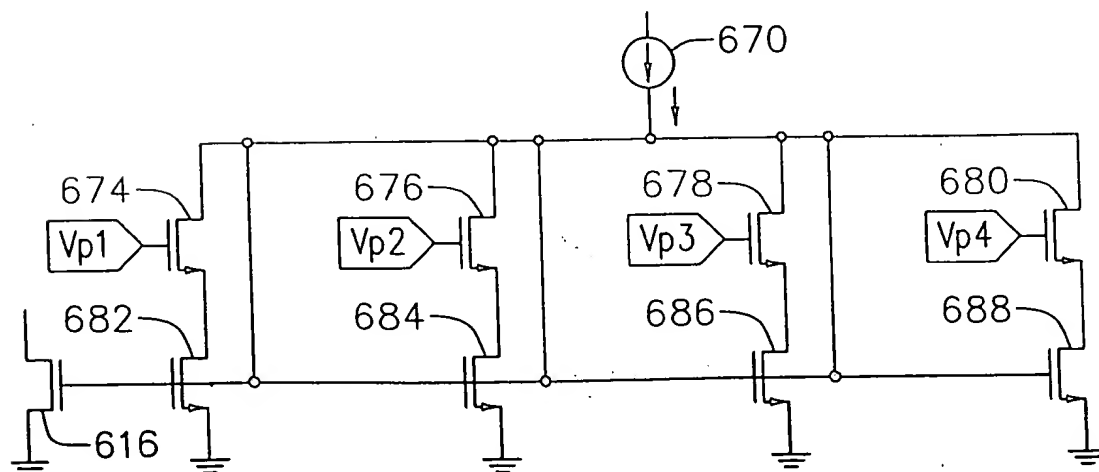


FIG.28



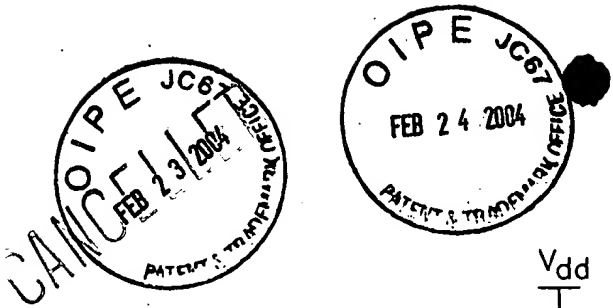


FIG.29

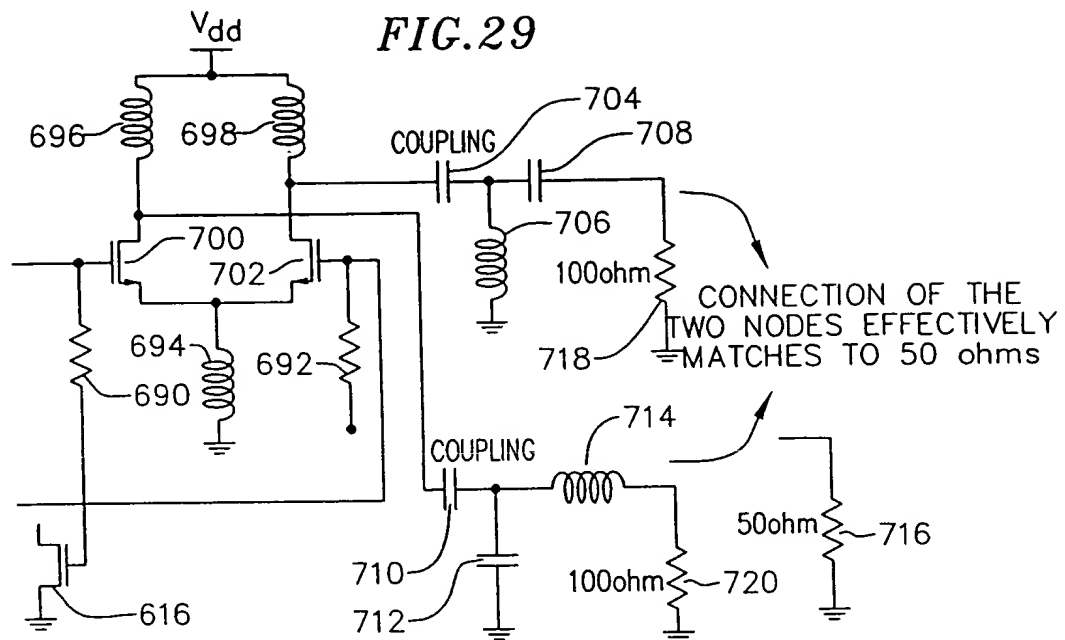
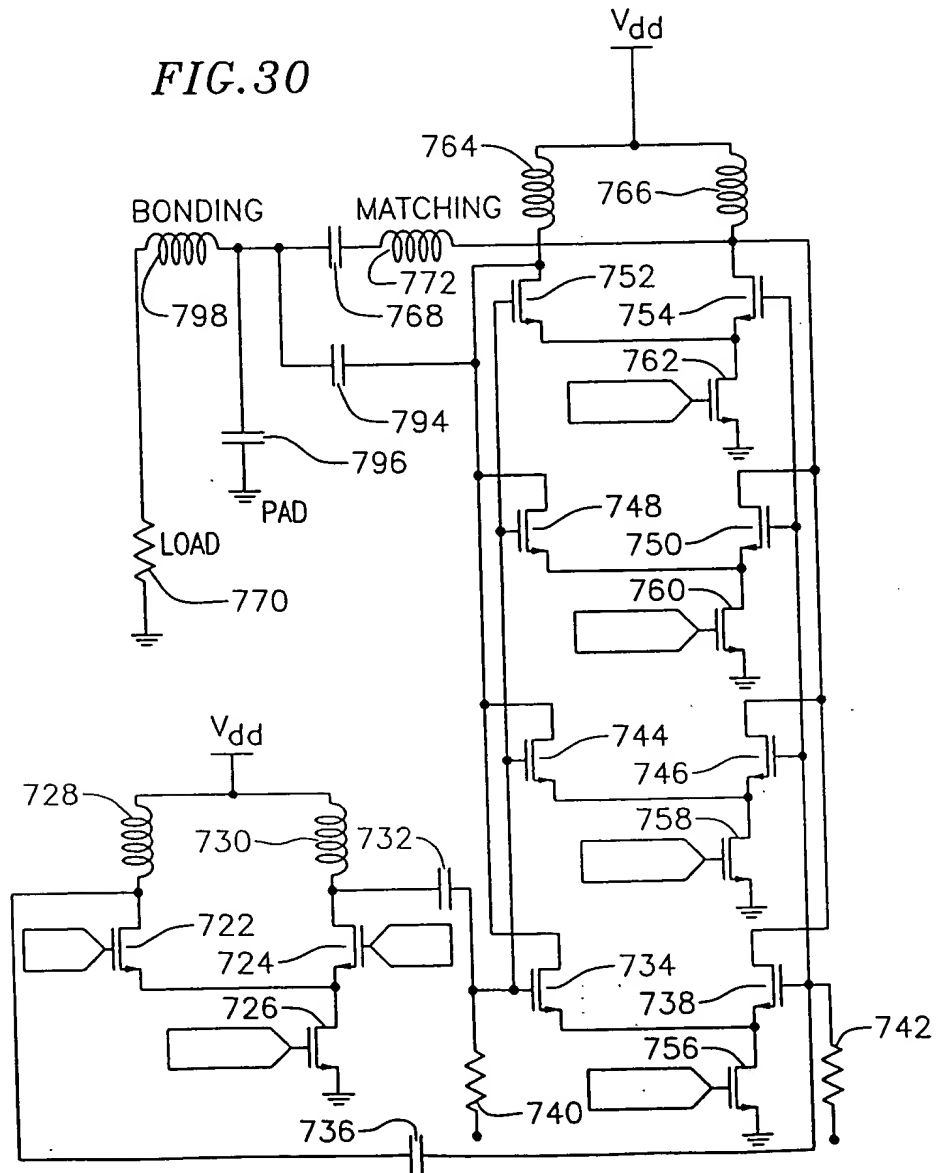


FIG.30



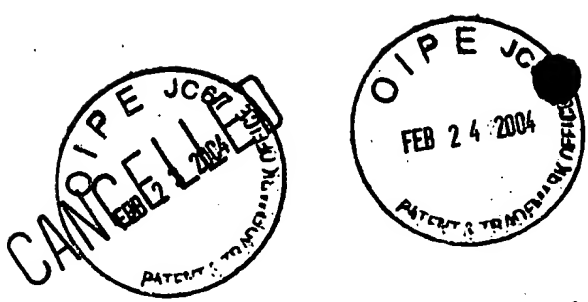


FIG.31(a)

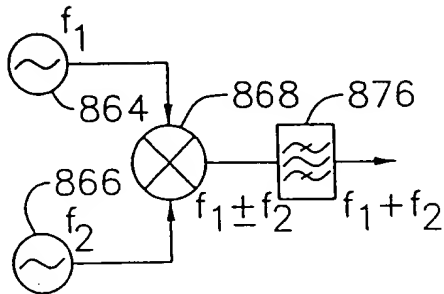


FIG.31(b)

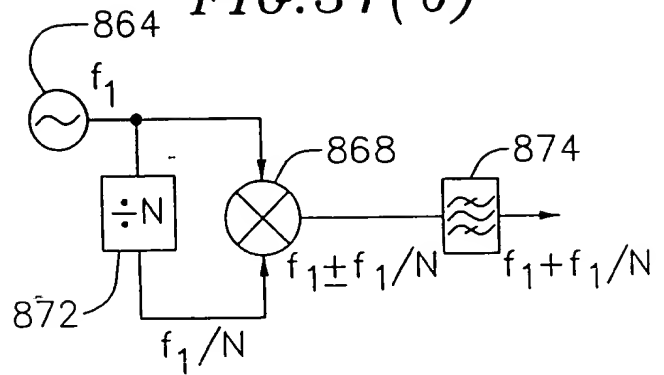


FIG.32

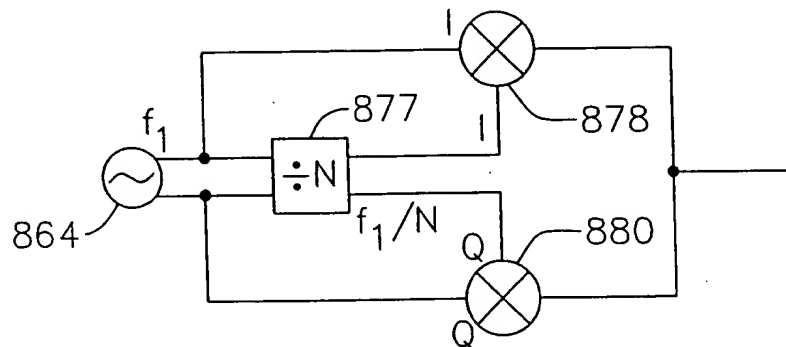
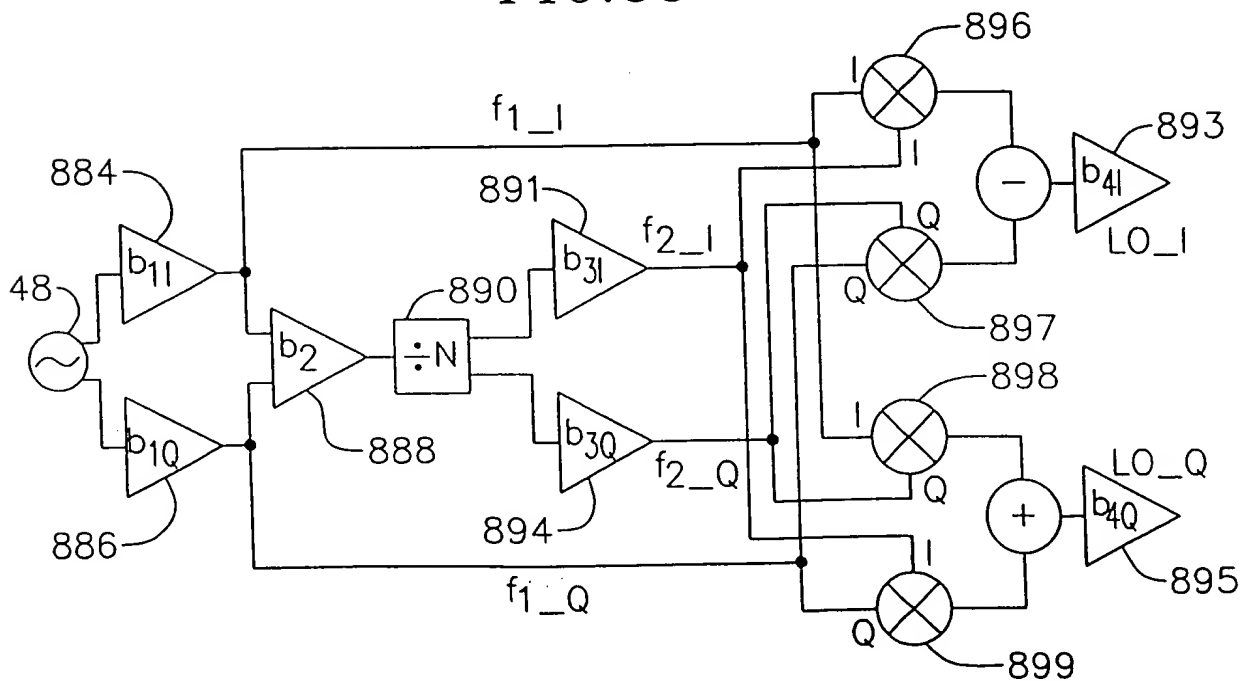


FIG.33



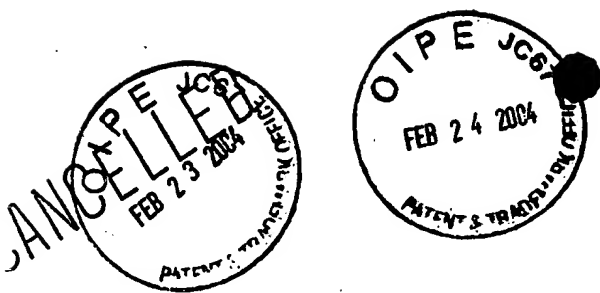


FIG.33(α)

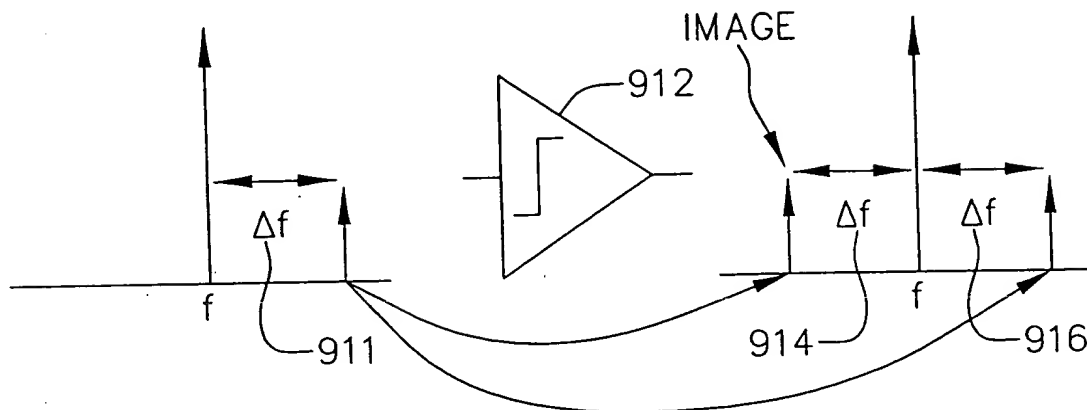
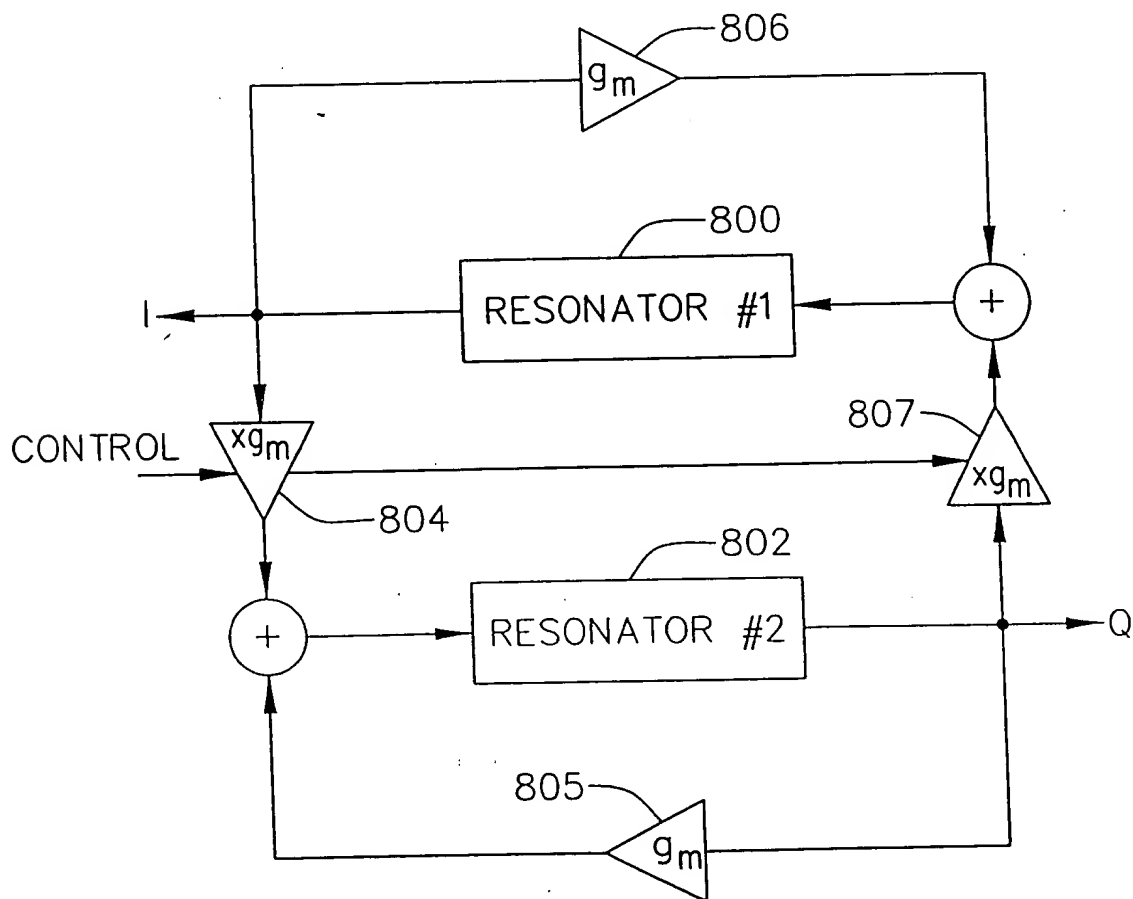


FIG.34



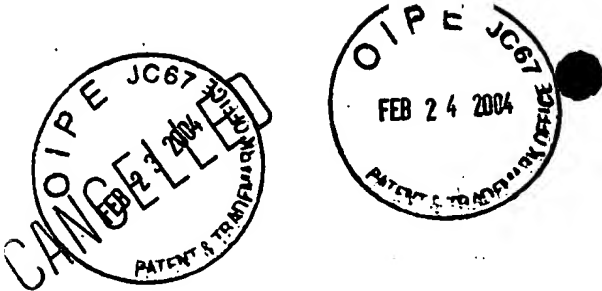
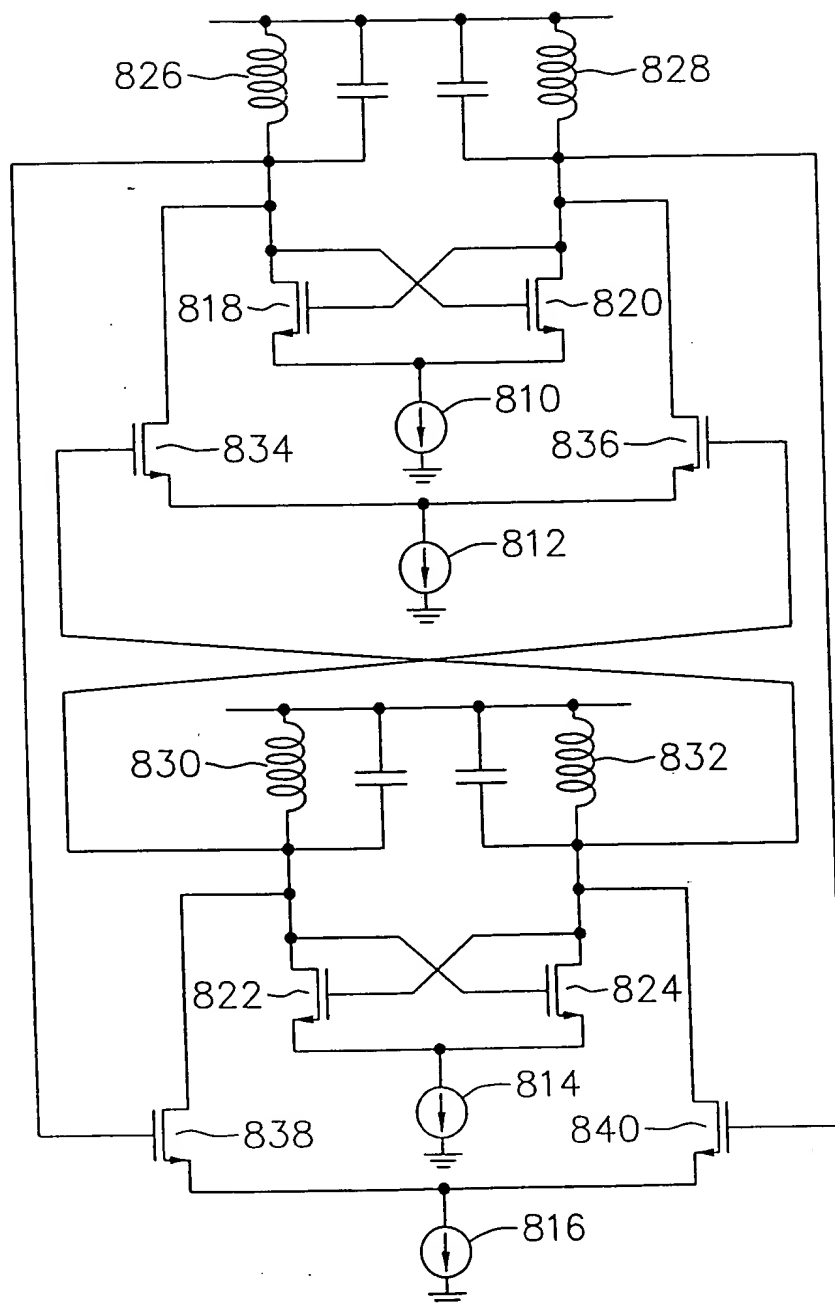


FIG.35



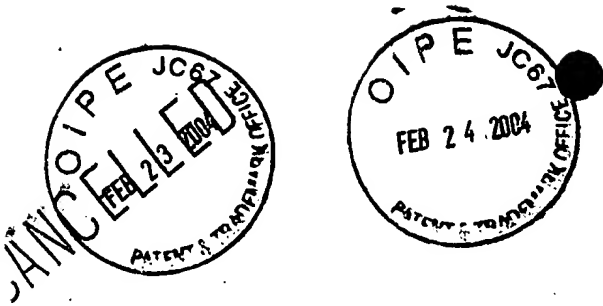
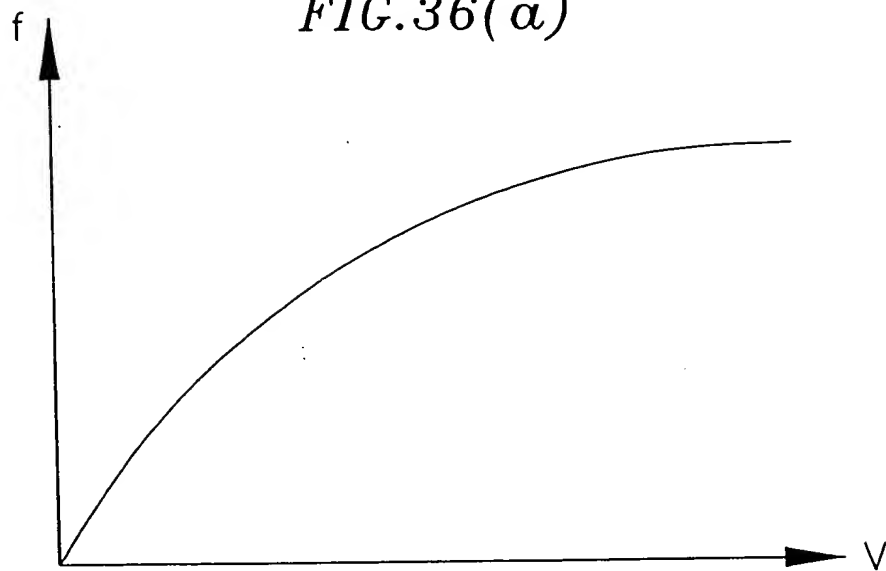
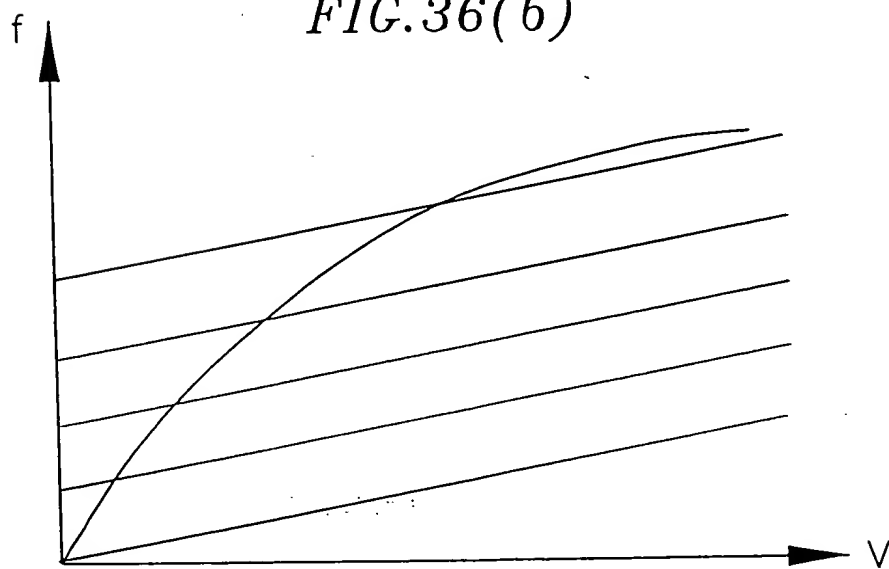


FIG.36(a)



TYPICAL VCO TUNING CURVE

FIG.36(b)



SEGMENTED VCO TUNING CURVE

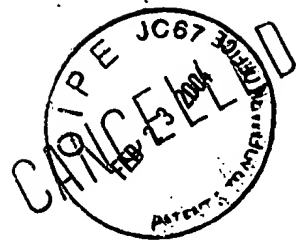


FIG.37(a)

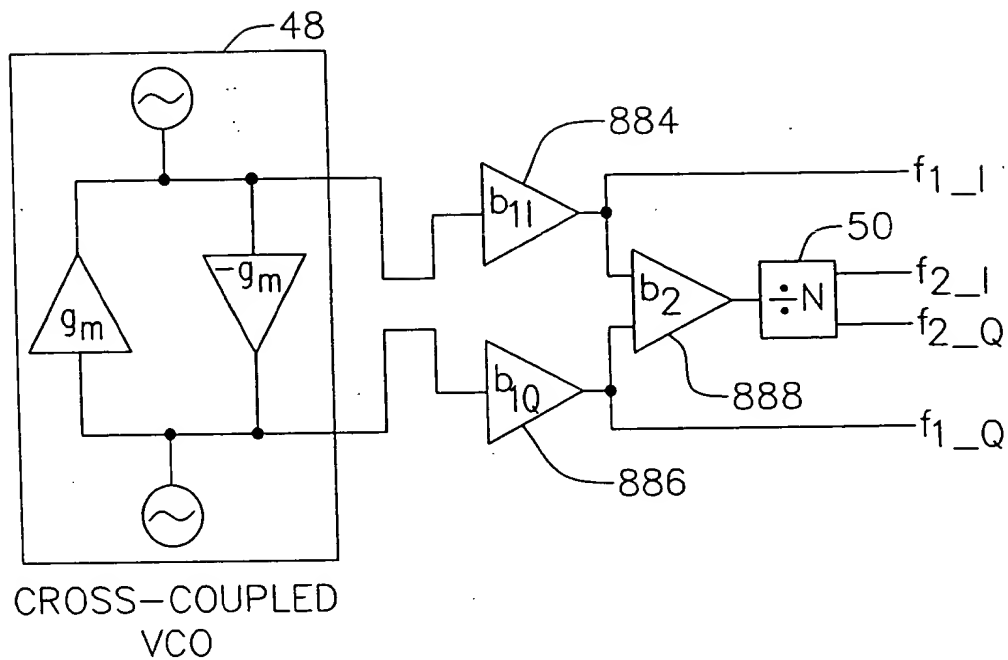
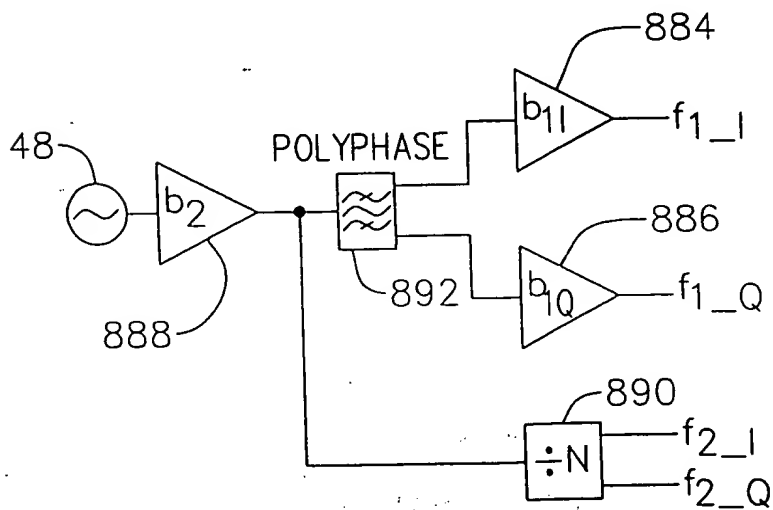


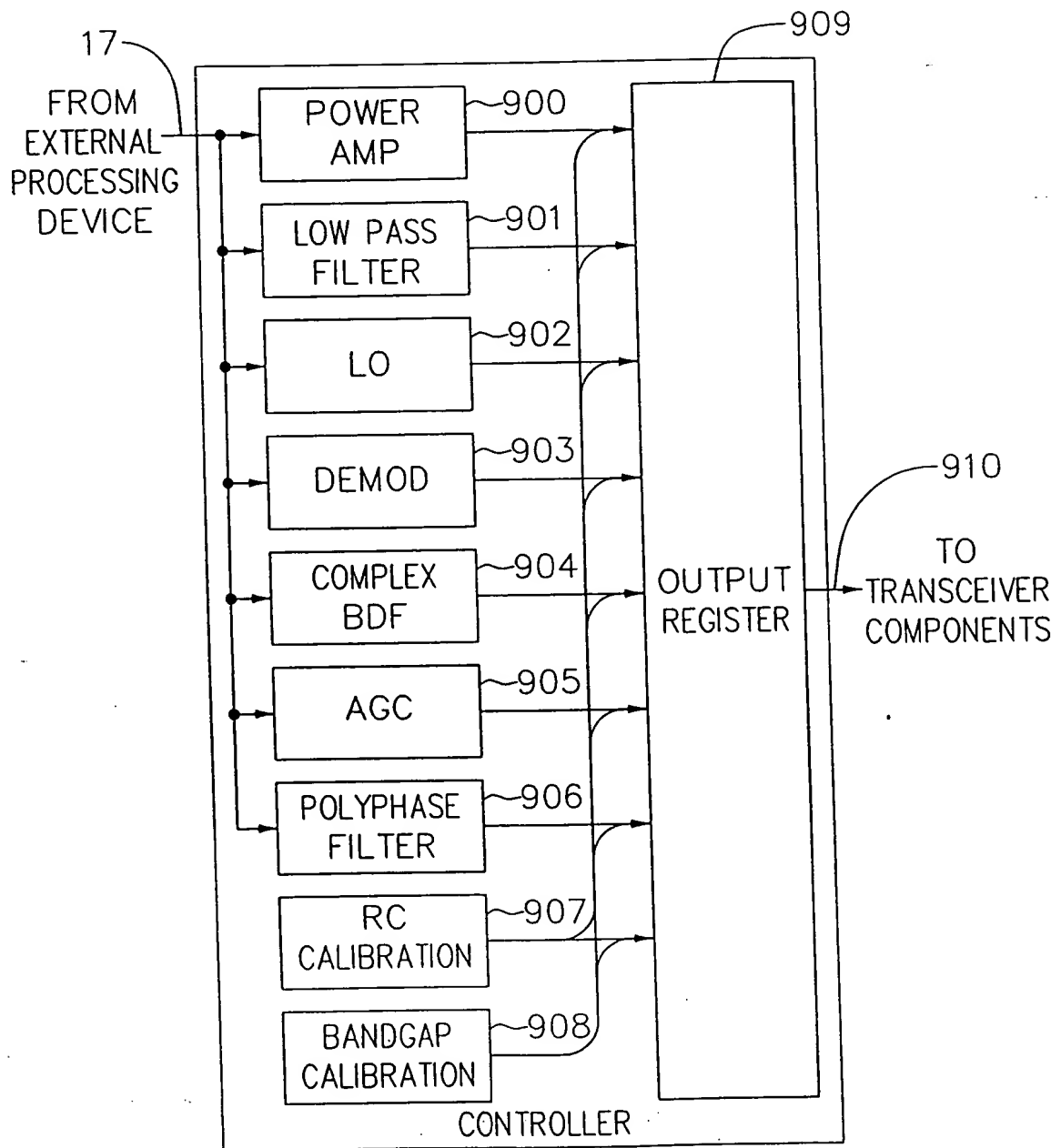
FIG.37(b)



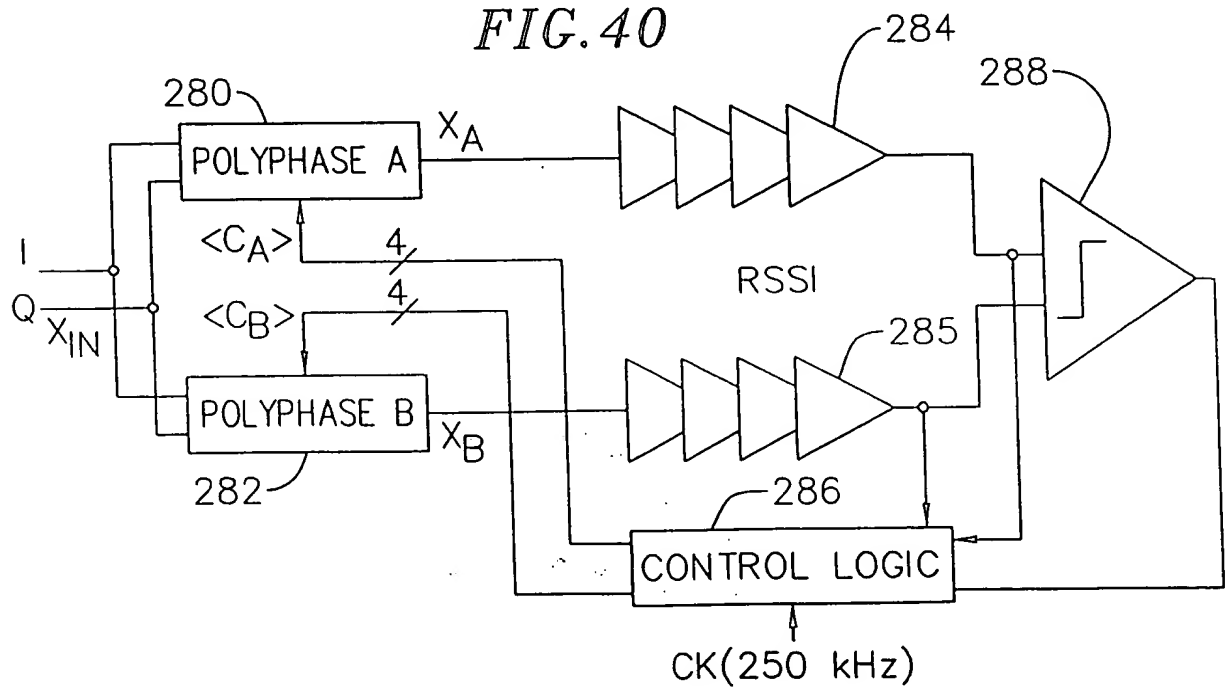
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FIG.38



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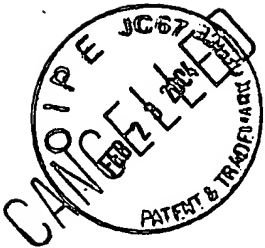


FIG. 41

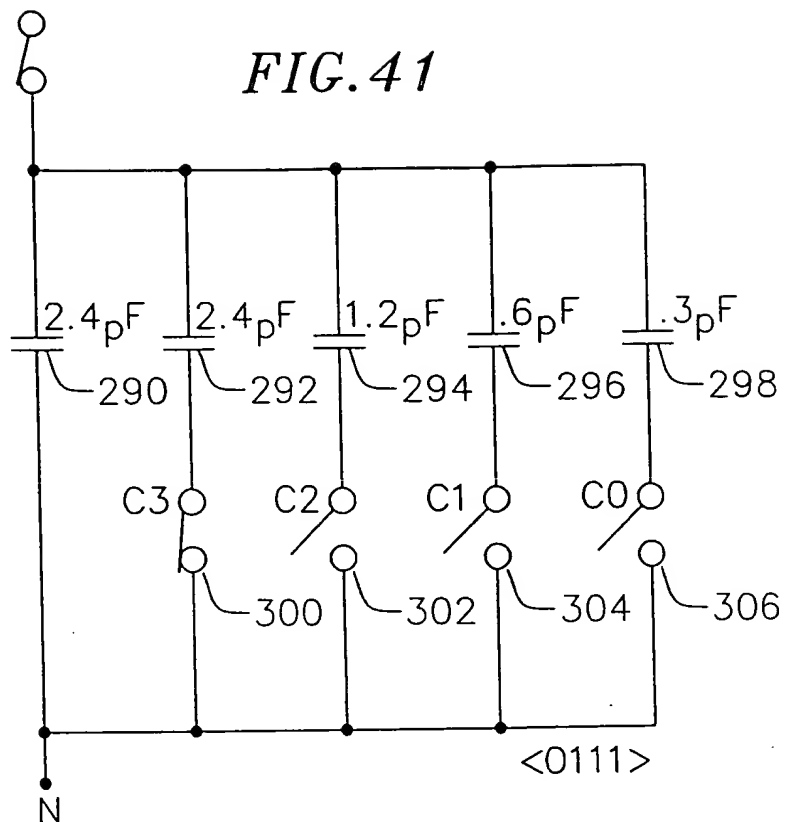
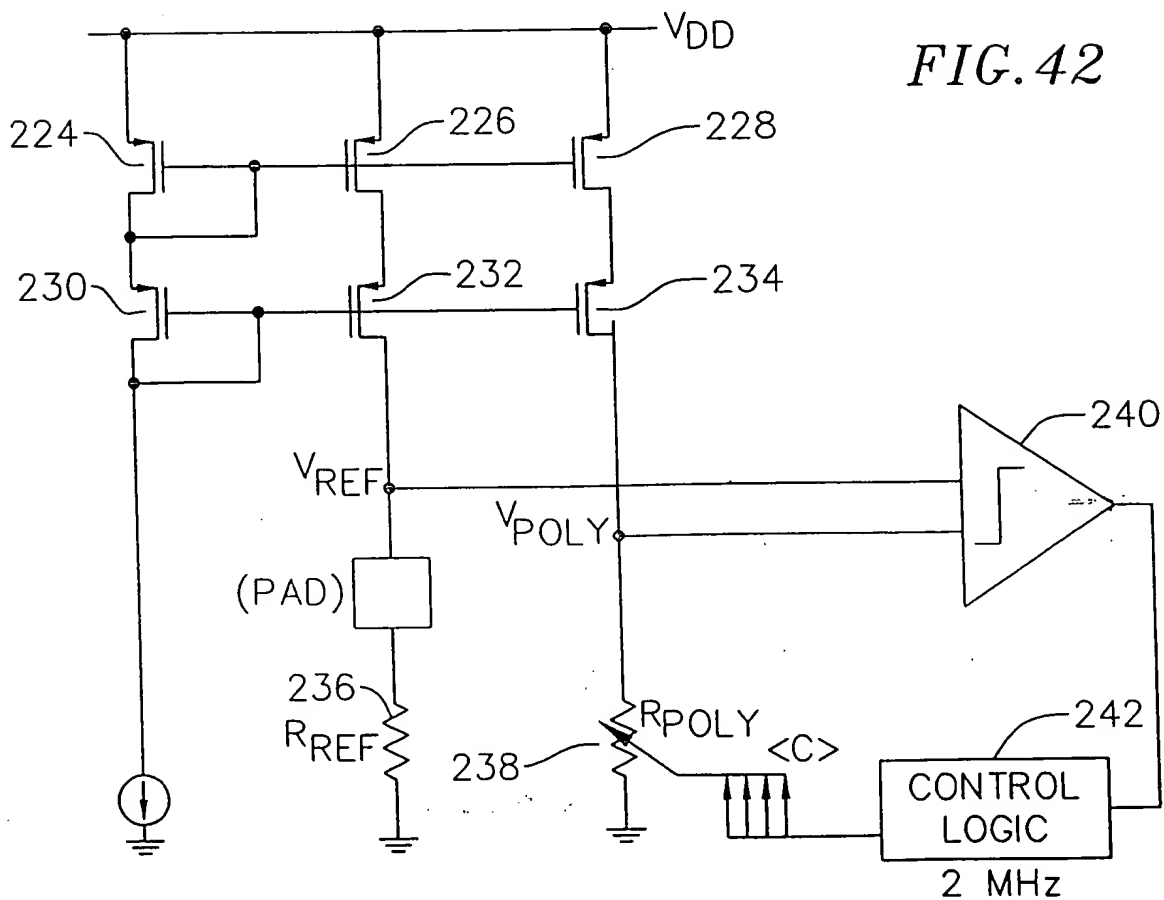


FIG. 42



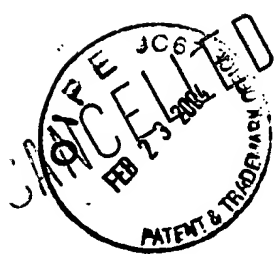


FIG. 43

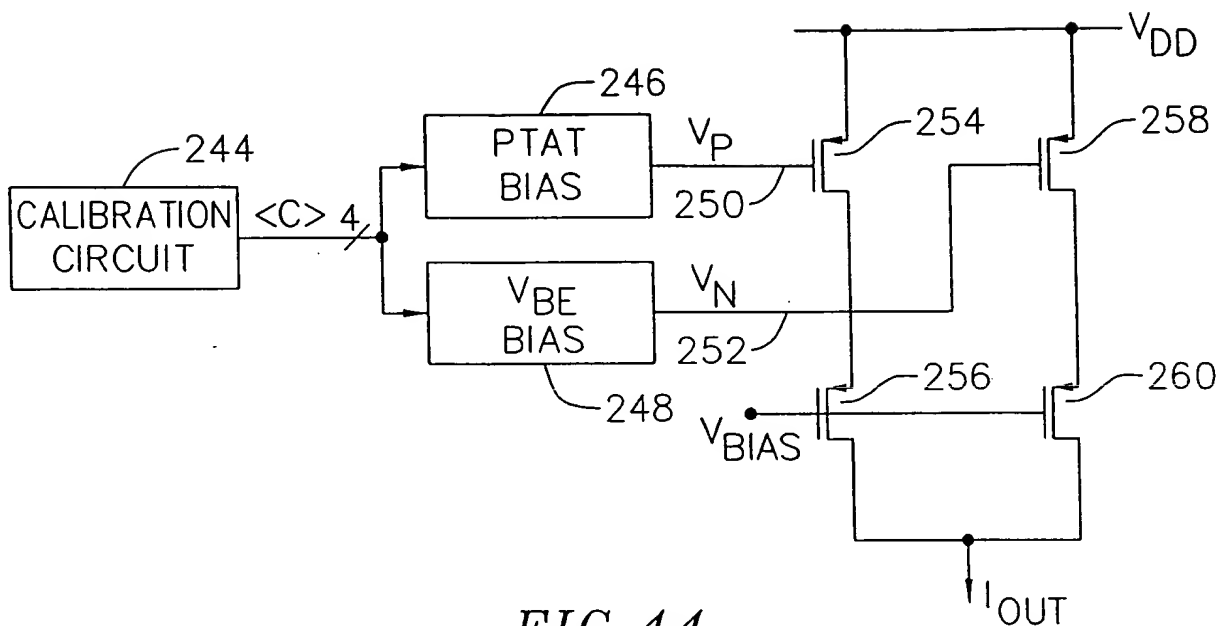


FIG. 44

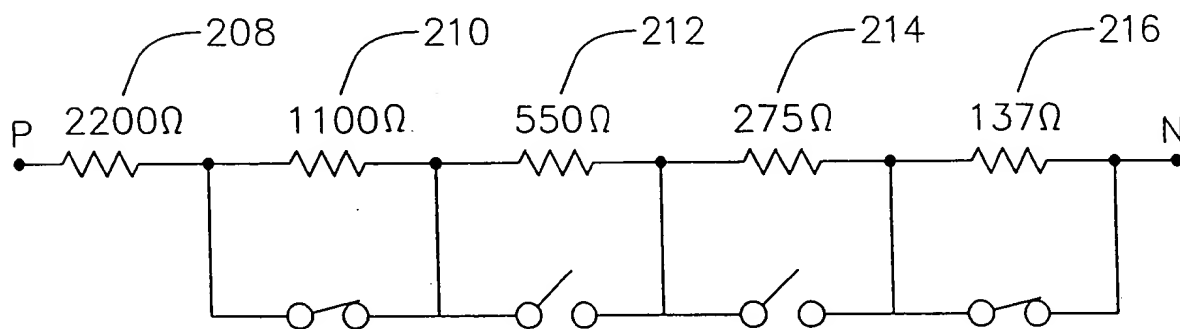
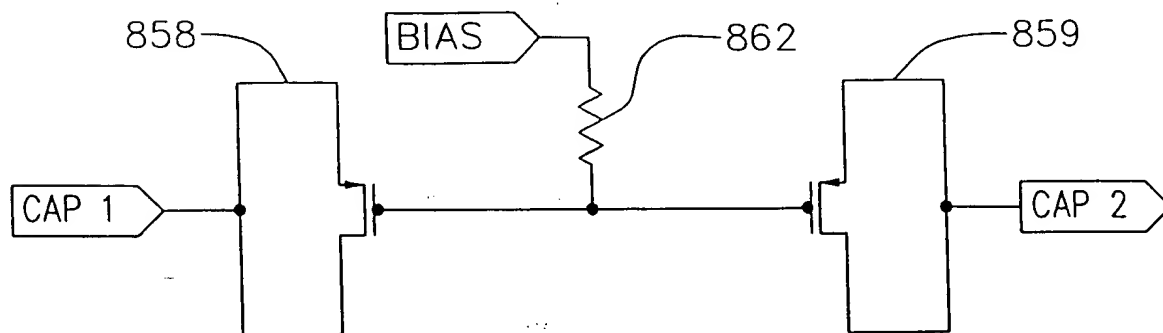


FIG. 45



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FIG. 46

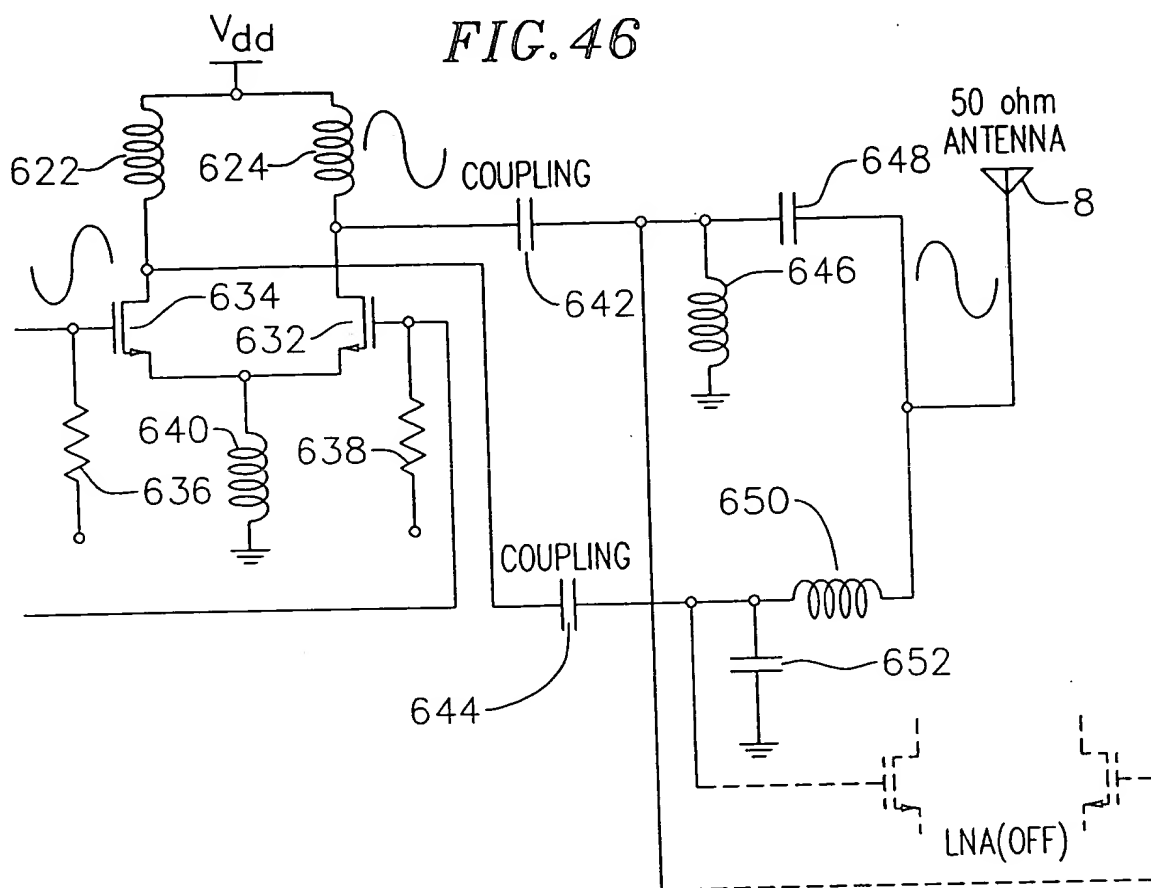


FIG. 47

